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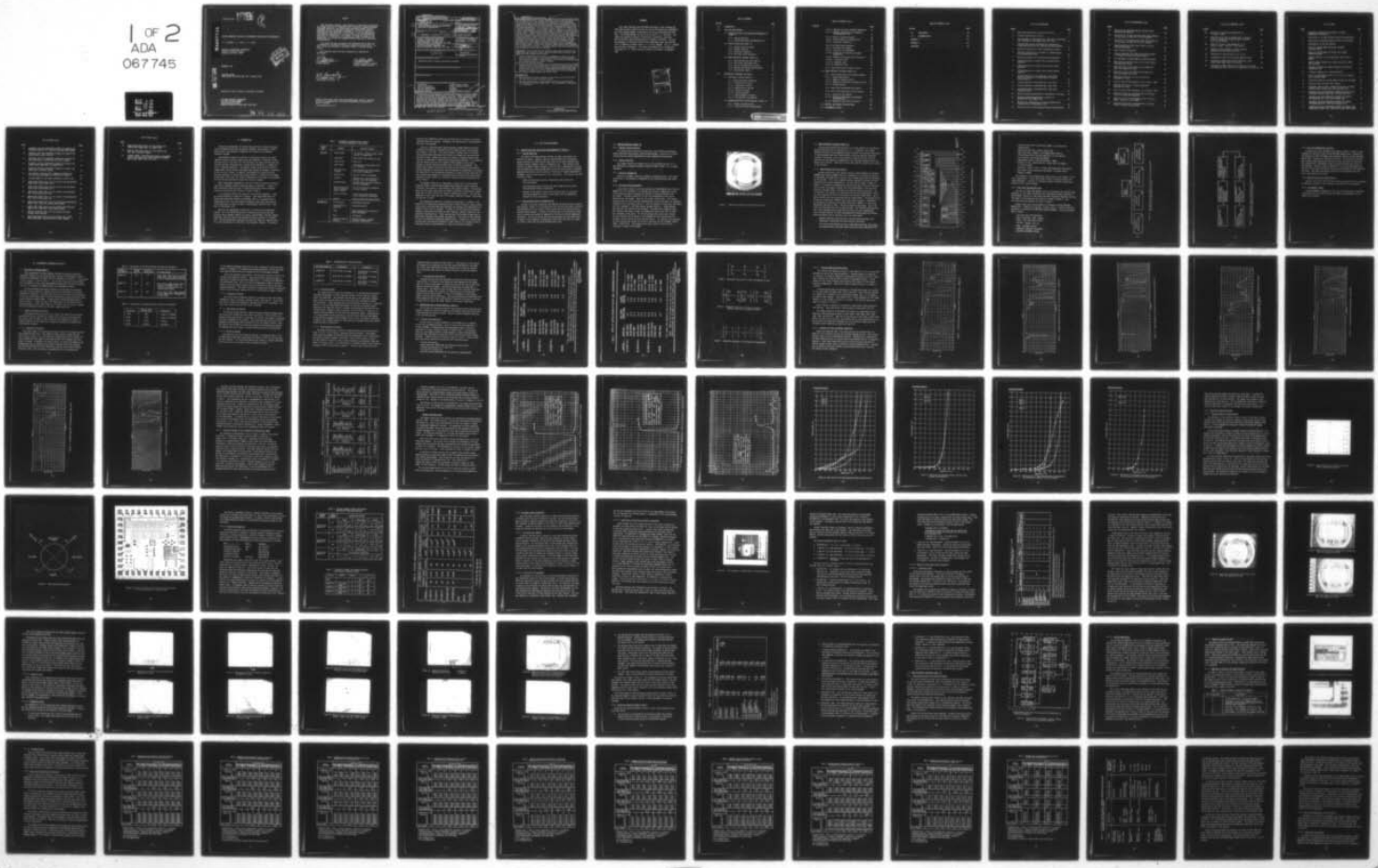

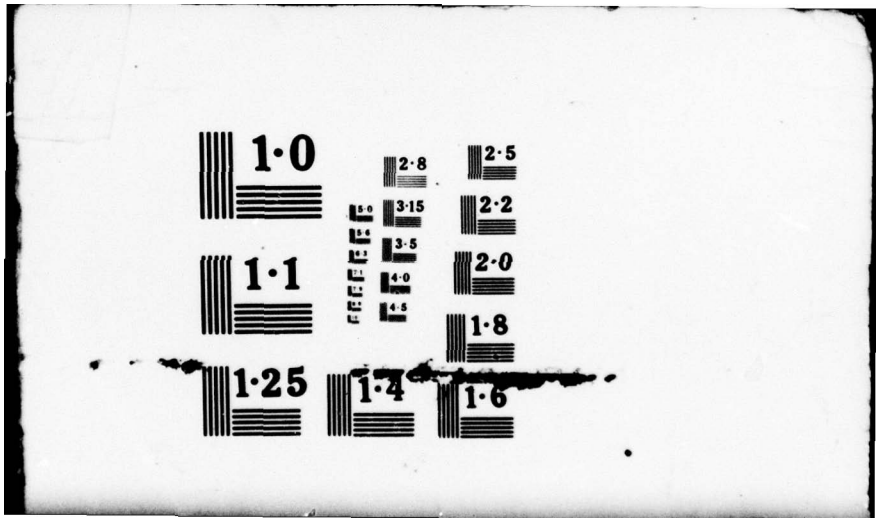
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LEVEL II

SOLVENT REMOVABLE COATINGS FOR CONTAMINANT PROTECTION OF MICROCIRCUITS

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ROCKWELL INTERNATIONAL CORPORATION
Electronic Devices Division
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NOVEMBER 1978

TECHNICAL REPORT
FINAL REPORT FOR PERIOD JUNE 1977 to AUGUST 1978

Approved for public release; distribution unlimited

AIR FORCE MATERIALS LABORATORY
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

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microcircuit	solvent soluble coating
hybrid microcircuit	solvent removable coating
particle contamination	silicone
particle immobilization	halocarbon
conformal coating	solvent strippable coating

minus 65°C plus 150°C

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this program was to develop and evaluate low molecular weight silicone and halocarbon polymers which are solvent removable for application to hybrid microcircuits for contaminant protection. Three experimental silicone waxes and four halocarbon waxes were selected for evaluation. The materials were chemically, thermally and electrically characterized. The stressing effects of these coatings on one-mil gold wire bonded to aluminized silicon die were determined by thermal cycling from -65°C to +150°C. Half of the wire bond samples were subsequently tested for moisture resistance per

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MIL-STD-883A, Method 1004.1, without bias. As a result of the wire bond, thermal and humidity tests, two coatings were selected for further evaluation. These coatings were a block copolymer of α-methylstyrene and dimethylpolysiloxane and a formulation of this same copolymer with a halocarbon wax. These materials were used to coat hybrid microcircuits containing devices sensitive to surface contamination. The coatings are easily removable for rework using trichlorotrifluoroethane in a two chamber immersion degreaser or a Soxhlet extractor. Reworked device and wire bonds showed no evidence of coating contamination effects. Conductive particles were added to one-half of the coated test hybrids prior to sealing. The test hybrids, together with uncoated controls, were then subjected to mechanical shock, constant acceleration, high temperature storage, and burn-in tests. No device failures and no wire bond failures attributable to the coatings occurred in any of the test hybrids. One mesa transistor failed after burn-in and one CMOS failed after mechanical shock — each device was in the uncoated control microcircuits. All of the coated hybrids passed particle impact noise detection (PIND) testing including those with particles added. Two out of 16 uncoated control hybrids failed PIND testing on completion of the tests. Preliminary material and process specifications were prepared for the two selected coatings.

CONCLUSIONS: After reverse bias and 1000 hour steady state life tests (first group); and after mechanical shock, constant acceleration and 1000 hour high temperature 150°C storage (second group):

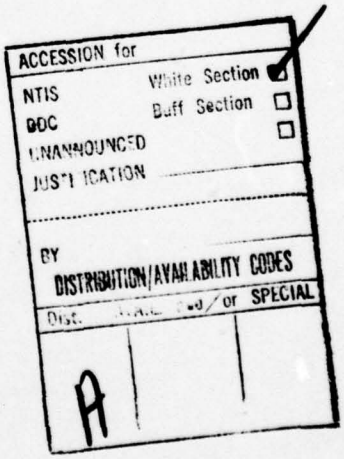
1) Except for Pd/Ag/Pd oxide resistors, no degradation of devices was found due to coating. Changes in the Pd/Ag/Pd oxide resistors were expected because palladium oxide is always extremely reactive and has long been used as a reduction catalyst in organic reactions.
2) No wire bond failures occurred.
3) Coatings provided particle protection and immobilization of particles added to hybrid microcircuits (half of coated circuits were seeded with particles). Coated circuits all passed PIND testing, while two uncoated microcircuits failed PIND testing (all circuits passed PIND testing after package seal). There was no evidence of particle induced failures in any of the hybrids.
4) All packages retained hermetic seals after tests.

RECOMMENDATIONS:

1) Coatings should be further evaluated on high density microcircuits used for functioning integral electronic systems.
2) Coatings should be used to insure higher reliability in microcircuits. This would be especially valuable where circuit replacement is impossible; e.g., satellites.

FOREWORD

This report describes work performed from June 1, 1977 to August 30, 1978 under Contract F33615-77-C-5141 for the Air Force Materials Laboratory, Air Force Systems Command, United States Air Force, Wright-Patterson AFB, Ohio. The Program Manager for the Air Force was Mr. E. J. Morrisey. This report was prepared by Rockwell International Corporation, Electronic Devices Division, Hybrid Microelectronics, Anaheim, California. The work was performed in the Special Microcircuits Department under the direction of M. W. McMurran, Director and Dr. J. J. Licari, Manager. Dr. B. L. Weigand was Principal Investigator. The report was prepared by Dr. Weigand with assistance by L. R. Schulz and was released by the authors in September, 1978.



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1.0 INTRODUCTION

Particulate contaminants of various types and from a variety of sources can be introduced during the fabrication, assembly, and packaging of hybrid microcircuits, and continue to jeopardize the reliability of expensive electronic systems.

The presence of metallic particles on microcircuit surfaces can cause immediate failures (usually caught during environmental or functional screening tests prior to sell-off), or, more seriously, can cause failures after the circuits have been installed into a system and are operating in a manned aircraft or unmanned spacecraft. For example, a small piece of wire initially lodged under a device could be dislodged later during the shipment or operation of the circuit or system. In general, the probability of metal particles shorting conductors or devices and causing failure is a function of the number of particles, their size, the circuit configuration, the volume of the packages, and the time and conditions to which the circuit is exposed.

Other contaminants (nonmetallic) can be as serious as metallic particles, resulting in leakage currents, electrical opens, or corrosion. A matrix of some contaminants which can occur in hybrid microcircuits and in packaged electronic devices and their sources is given in Table 1.

It is extremely difficult to clean off all particles completely — many are electrostatically or physically attached. Even though PIND (Particle Impact Noise Detection) testing is performed, there is no guarantee that a lodged particle will not later become dislodged or that other particles may not be generated as a result of wear or metallurgical corrosion over a long shelf or operational life.

There are two complementary approaches to resolving the contamination problem. One is to define the sources of deleterious particles and then establish design changes, material or process substitutions, improved cleaning procedures, stricter controls and thorough testing to minimize or eliminate them. The second approach, assuming that there will always be some particles, is to coat the device or circuit with a thin polymeric coating. The coating

TABLE 1. CONTAMINANT CATEGORIES/TYPES/SOURCES IN HYBRID MICROCIRCUITS AND DEVICES

General Type	Example	Possible Sources
Metallic	Pb/Sn Solder	Lid sealing, solder plating, solder terminal on capacitors
	Kovar/Gold	Weld splash from sealing to cans
	Gold slivers	Gold wire
	Gold Flakes	Burnishing of bonding pads prior to TC bonding
	Gold particles (flakes)	Electroplated gold from package, lid, circuit conductors
	Gold/Silicon	Eutectic from die attachment
	Aluminum	Aluminum wire, metallization on devices, thin film conductors
	Nickel/Chromium	Nichrome resistors from mechanical resistor adjustments
	Resistor particles such as Ruthenium oxide, iridium	Thick film resistors, mechanical or laser scribing
	Silver particles	Silver-filled epoxy adhesives, silver terminals on capacitors
	Gold/Sn	Preform splash from seam sealing
Non-Metallic	Silicon chips	Semiconductor devices
	Alumina/beryllia particles	Substrate material
	Epoxy	Epoxy adhesives for substrate or device attachment
	Flux	Lid Sealing
	Corrosive chemical residues	Cleaning solvents, etching solutions, photoresists

would not only immobilize particles, but would act as a barrier to particles generated during lid sealing. Ultimately, the combination of both approaches may have to be employed.

The use of coatings within hybrid packages, though appealing from the standpoint of attaining "foolproof" particle immobilization, has presented two problems in the past. The normal polymeric coatings such as silicones and p-polyxylylenes (Parylenes) are difficult to remove once they have been applied or cured. Because the repair and rework of expensive hybrid microcircuits are important in reducing costs and meeting schedules, it is essential that any coating used be easily removed without damage to the circuit. Secondly, coatings should be assessed from a reliability standpoint. The effects that coatings can have on the large variety of devices and interconnections employed in microcircuits must be measured and determined to be benign. The objectives of this program were therefore to select coatings that could be easily applied and removed in a manufacturing environment and to assess these coatings for their effects on a variety of sensitive active and passive electronic devices.

The approach taken was to investigate a unique class of low-to-medium molecular weight, uncrosslinked polymers which; because of their molecular structures, are soluble in conventionally used organic solvents. The coatings which are most widely used today are highly crosslinked, high molecular weight types and, as such, difficult to remove in reworking a circuit. The coatings addressed in this study consisted of silicones, modified silicones, halocarbons and mixtures of these.

The program was conducted in essentially three phases. In Phase I, the feasibility of applying and reworking solvent soluble coatings on reject hybrid microcircuits was established and experience was gained on the application and removal of this class of coatings. In Phase II, the silicones and halocarbon coatings selected were evaluated for their chemical, thermal, electrical, and mechanical characteristics. Those coatings that did not meet minimum requirements were eliminated from further consideration. The effects of the coatings on fine wire bonds were determined quantitatively. In Phase III, the best two coatings were selected and evaluated for their effects on a variety of active and passive devices interconnected in a hybrid microcircuit assembly.

2.0 TEST PLAN AND APPROACH

2.1 COATING SELECTION, APPLICATION AND REWORKABILITY (PHASE I)

2.1.1 Coating Selection

The highly crosslinked polymer coatings, by their very nature, are difficult to rework. However, there are uncrosslinked and low molecular weight variations of these coating types which can be easily removed using cleaning solvents commonly used in a production line. These belong to the classes of synthetic waxes; oligomers, and gel-like or elastoplastic coatings. This new approach of using coatings that can be dissolved quickly in standard manufacturing solvents such as toluene or Freon and in standard manufacturing equipment, such as vapor degreasers, was investigated. The coatings that were selected included:

- Three silicone waxes specially formulated by Dow Corning for this application.
- Four halocarbon waxes selected from those commercially available from Halocarbon Products Corporation.
- Mixtures of the above silicone and halocarbon waxes to reduce the moisture permeability of the silicone and/or the low temperature flexibility of the halocarbon.

2.1.2 Coating Application and Reworkability

Solvents to be used in applying and removing the coatings were evaluated and selected. Reject F-111 and other thin film circuits were used to evaluate the reworkability of the circuits after application of the coatings and subsequent coating removal. Mixtures of the waxes were also evaluated as necessary to achieve the optimum low temperature flexibility and high temperature properties. This was to ensure that the coating would not flow sufficiently to expose circuit elements at temperatures below 150°C and would not become so rigid at -65°C that wire bond breakage would occur.

2.2 COATING EVALUATION (PHASE II)

2.2.1 Chemical Characterization

The coatings were characterized chemically using infrared spectroscopy, atomic absorption spectroscopy, emission spectroscopy, titration for chloride ion, and molecular weight determination by gel permeation chromatography.

2.2.2 Thermal Stability

The thermal stabilities (weight loss) of the coatings selected in 2.1.1 were determined by thermal gravimetric analysis (TGA) to 450°C, in a nitrogen atmosphere.

2.2.3 Electrical Properties

Dielectric strength, dielectric constant, dissipation factor, and volume resistivity of the coatings or components of the coating mixtures were determined.

2.2.4 Wire Bond Stress Evaluation

A test matrix similar to the one designed for Army/MIRADCOM under Contract DAAK40-76-C-1117 (reference 1) to evaluate the effect of temperature cycling on wire bonds was used to evaluate the effects of coating stresses on the wire bonds. The matrix consists of a thin film aluminized silicon die to which Au wires are bonded. These die are 0.200 x 0.200 inches. This configuration allows for fast electrical determinations and also provides for diagnostic evaluation of an individual bond pair. Each die contains 42 bond pairs (84 bonds). The die is mounted in a 42-lead ceramic package (Figure 1). Eight packages were used for each coating to be evaluated. The bonds were nondestructively pull tested to two grams, coated, and temperature cycled from -65°C to 150°C for a minimum of 100 cycles. All of the packages were electrically tested for bond failures and the bonds on four packages for each coating were pull tested to failure before and after coating removal. The remaining four packages for each coating were tested for moisture resistance per MIL-STD-883A, Method 1004.1, without bias. The packages were again tested for bond failures, corrosion, or other failure modes.

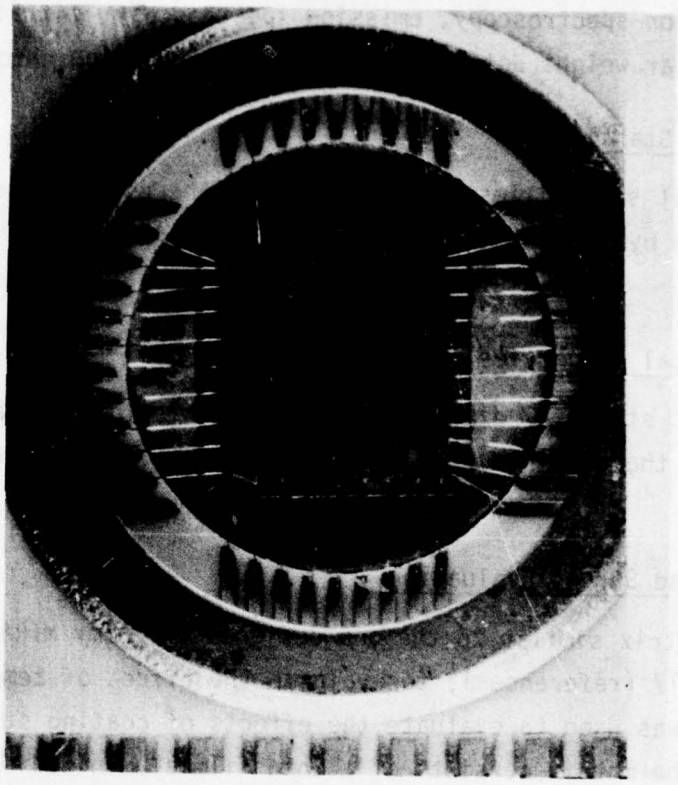


Figure 1. Bond Stress Evaluation, 42-Lead Test Circuit

2.3 QUALIFICATION OF COATINGS (PHASE III)

Two coatings selected from the tests in 2.2 were applied to a minimum of 46 hybrid microcircuits as described in 2.3.1. In addition, 18 of these hybrid microcircuits were assembled without coatings; the electrical properties of these packages were fully characterized to serve as baseline references. Sixteen of the coated circuits were purposely seeded with solder and gold particles for the purpose of determining if the coatings actually protect the devices and circuitry. These test circuits were used for qualification testing of the coatings.

2.3.1 Hybrid Microcircuit Test Vehicle

A hybrid microcircuit test vehicle similar to that designed for the Army/ERADCOM under Contract DAAB07-76-C-1310 (reference 2) to evaluate the effects of outgassing from adhesives on hybrid circuit elements was used for evaluation of the coatings. This circuit contains devices especially selected for their sensitivity to surface contamination. The test circuit layout is shown in Figure 2. Resistors R1 through R4 are PdAg-Pd oxide thick film chip resistors. The circuitry is designed to permit four point measurement of the low value resistors (450 ohms $\pm$20%) to minimize the effect of contact resistance. Two of the thick film resistors are glassivated and two are unglassivated. Resistors R5 through R8 are thin film nichrome chip resistors (500K ohms). Two of these resistors are also glassivated and two unglassivated. Transistors Q1 and Q2 are mesa transistors, 2NC5975, with unpassivated junctions. Transistors Q3 through Q6 are junction field effect transistors, 2N4391. Z1 and Z2 are operational amplifiers, LM741. The two op amps are glassivated. Two of the JFETs are glassivated and two are unglassivated. The interdigitated capacitor has 2.5 mil spacings and was used for insulation resistance measurements. Thin film metallization is plated gold/evaporated nickel/evaporated nichrome. Parts and devices used in the test circuit are given below:

- PdAg/Pd oxide thick film resistors (450 ohms $\pm$20% resistance, 500 ohms/square, glassivated and unglassivated, chip type).
- Thin Film nickel-chromium resistors (500K ohms resistance, glassivated and unglassivated, chip type, Hybrid Systems Part No. UHR-5E-500-3-N).

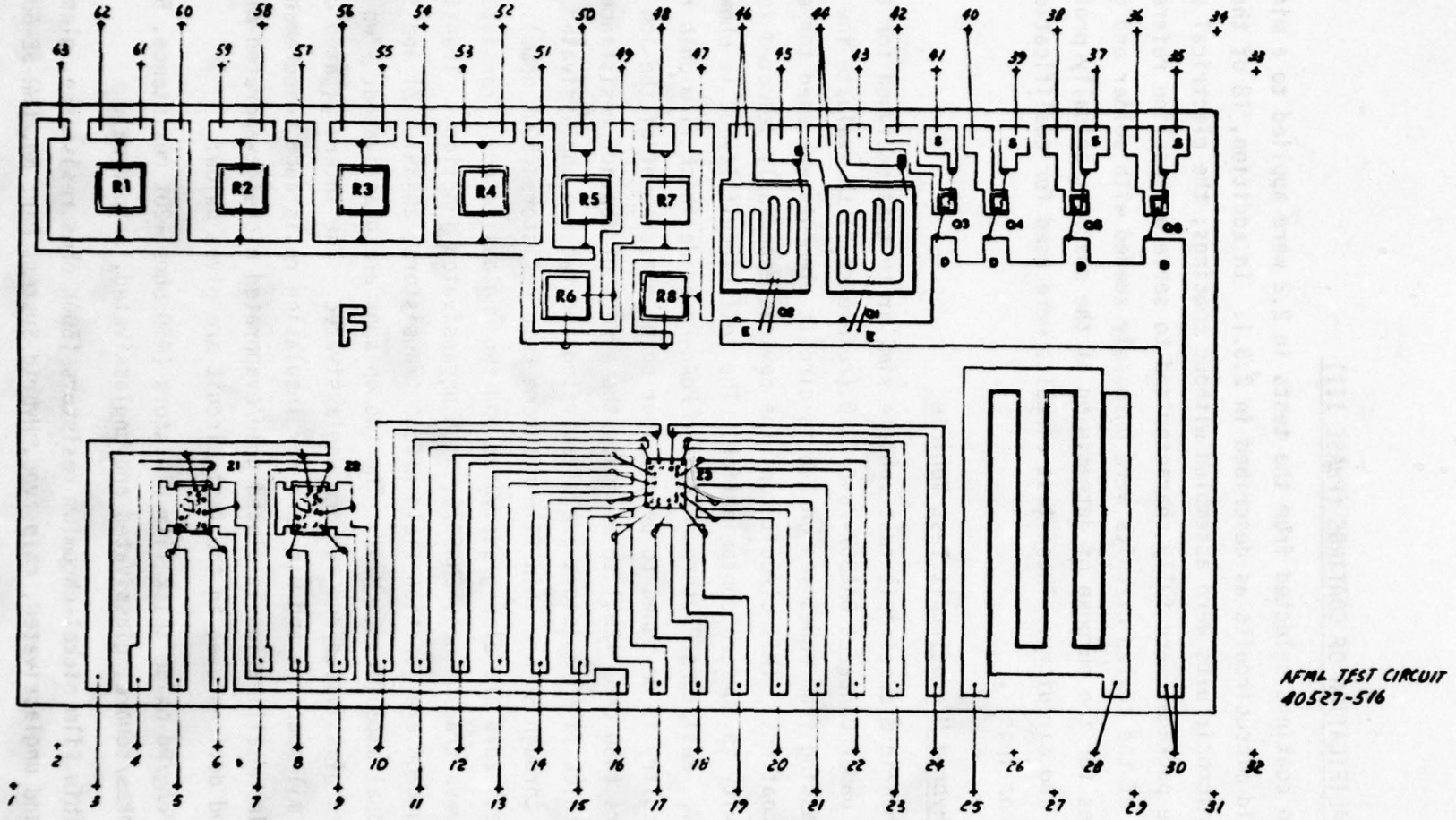


Figure 2. Coating Evaluation Test Circuit

- Junction field effect transistors, 2N4391, glassivated and unglassivated
- Operational amplifiers, LM741, glassivated
- Mesa transistors, 2NC5975, with unpassivated junctions
- Interdigitated thin film gold capacitor, 2.5 mil spacing — for insulation resistance measurements
- Complementary metal oxide semiconductor, CD4001
- Package, 63 pin, Tekform Part Nos. 35019, 35021 and 35029-2, to be seam sealed.
- Substrate, 1.600" x 0.775" x 0.027", MRC superstrate, 99% alumina
- Wire bonds, using aluminum and gold wires, ultrasonic and/or thermally bonded

The package is a gold-plated Kovar, 63-pin plug-in, of "uniwall" (solid ring) construction. It was sealed using a gold-tin preform on SSEC seam sealer equipment. Circuitry is designed to permit individual biasing and testing of each circuit element.

2.3.2 High Stress Accelerated Tests

Two sets of coated test samples (one set per coating) plus controls were subjected to high stress accelerated test conditions currently specified in MIL-STD-883B. One-half of the coated specimens contained conductive particles. The number of test specimens and controls is shown in Figure 3. The test conditions and sequence are shown in Figure 4.

Hermetic leak tests were performed in accordance with MIL-STD-883A, Method 1014.1, Condition A_2 (30 psig, 3 hours), and C_2. Particle tests were performed in accordance with NASA MSFC Drawing 16A02003. Electrical measurements included:

- Thick and thin film resistance
- Mesa transistors: Beta, leakage
- JFETs: Zero gate drain current
- Op Amps: V_{OFFSET}, I_B^+, I_B^-
- CMOS: Quiescent current
- Conductor insulation resistance
- Conductor breakdown voltage

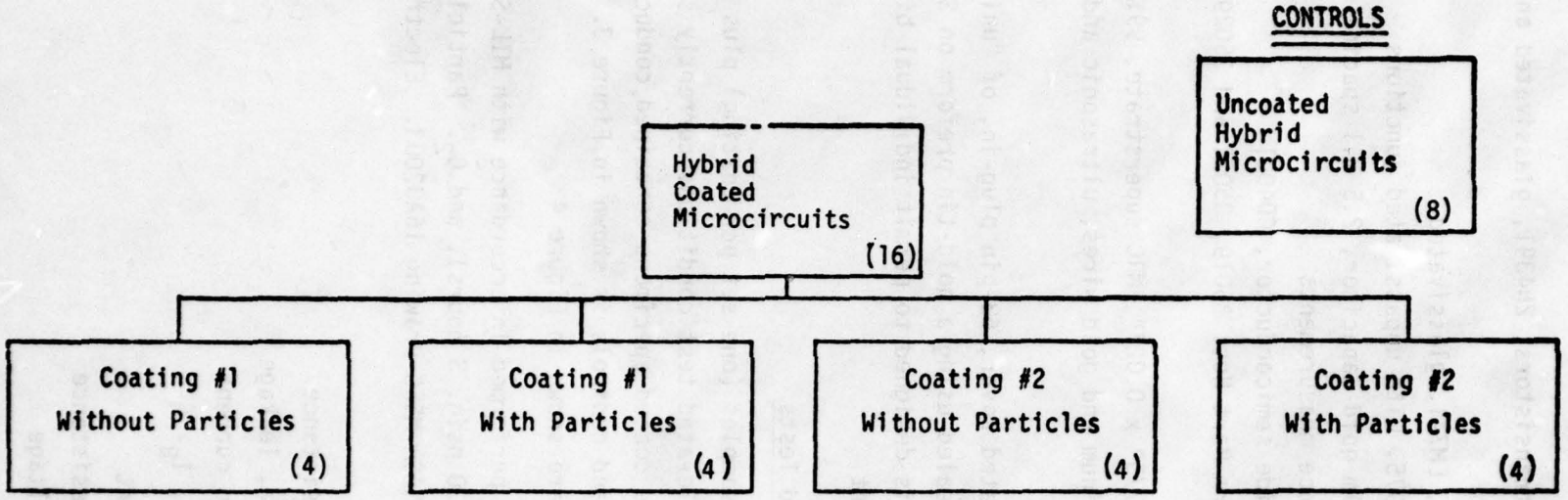


Figure 3. Test Specimen Lot Distribution for High Stress Accelerated Tests and Burn-in and Steady State Life Tests

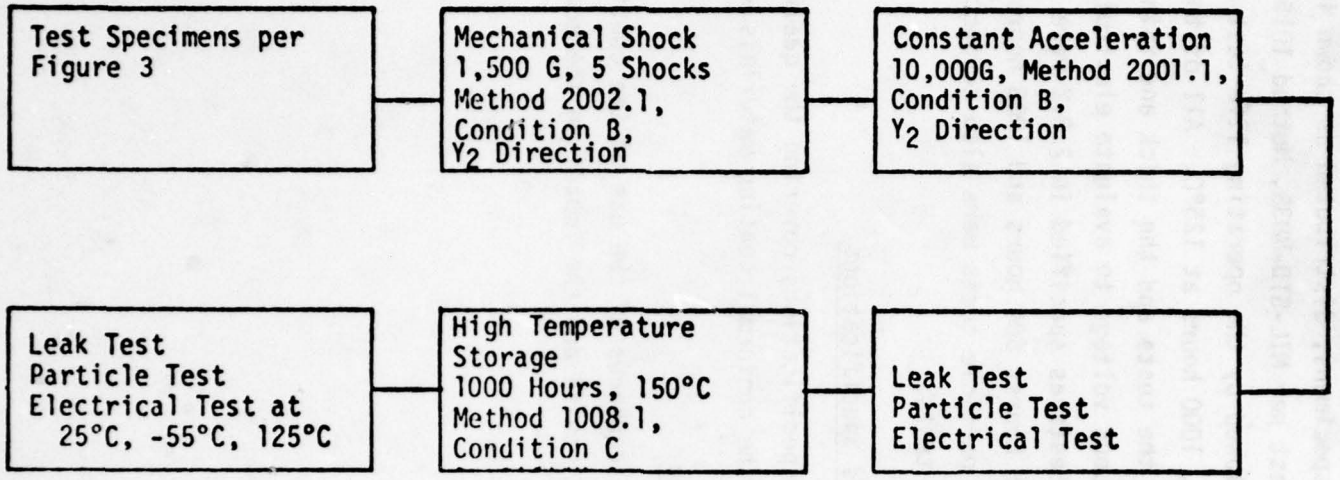


Figure 4. Proposed High Stress Accelerated Test Sequence for Coated Hybrid Microcircuits (Methods per MIL-STD-883B)

2.3.3 Burn-In and Operating Life Tests

A second set of test specimens, distributed as shown in Figure 3, were subjected to the burn-in test per MIL-STD-883B, Method 1015.2, Condition A, for 240 hours at 125°C followed by the operating life test per MIL-STD-883B, Method 1005.2, Condition A, 1000 hours at 125°C. All of the active devices were reverse biased during the tests and the thick and thin film resistors were subjected to a continuous voltage to evaluate electrolytic effects of the coatings. Electrical tests as specified in 2.3.2 were performed after the burn-in test and at 168 hours, 504 hours and 1000 hours for the operating life test. Leak tests and particle tests were also conducted after the burn-in and operating life tests.

2.3.4 Material and Process Specifications

Material and process specifications covering the qualification, acceptance, processing and control of the conformal coating materials were prepared.

2.3.5 Environmental Impact

The environmental consequences of the use of the coatings on production sized quantities of microcircuits and the impact on the economics of the process was evaluated.

3.0 EXPERIMENTAL PROCEDURES AND RESULTS

3.1 SELECTION OF COATING (PHASE I)

Three experimental silicone coatings from the Dow Corning Corporation (Midland, Michigan) and four halocarbon wax coatings from Halocarbon Products Corporation (Hackensack, NJ) were initially selected for evaluation. A description of the silicones is given in Table 2. Two of the silicone coatings (DC-E2907-43-1 and E2907-47-1) are linear polydimethylsiloxane while the third (DC-E2907--44-1) is a co-polymer of α-methylstyrene and polydimethylsiloxane.

The four halocarbon waxes were selected to be used alone or formulated with the silicone coatings to improve the electrical and moisture resistance properties as necessary. The halocarbon waxes are low molecular weight polymers of chlorotrifluoroethylene which have been separated by vacuum distillation into several molecular weight ranges. A description of these halocarbon waxes is given in Table 3. Except for one of the halocarbons, all the materials were selected because of their high solubility in Freon TF and in xylene or toluene, their high temperature stability, and their reported purities.

3.1.1 Rework and Repair Evaluation

A preliminary study was carried out to assess the feasibility of coating hybrid microcircuits, the ability to rework the circuits by dissolving away the coating, and the effect of the coating on 1-mil diameter wire bonds. A further objective of this phase was to establish procedures for applying and processing the coatings.

3.1.1.1 Selection of Circuits

Sixty (60) reject F-111 hybrid microcircuits (thin-film nichrome resistors/gold conductors) were used. The vintage of these circuits ranged from two years to over 10 years. All wire bonds were nondestructively pull tested; the 1-mil diameter gold wire bonds at two grams and the 2-mil diameter gold wire bonds at 6 grams. In addition, for most circuits, six gold wires bonded to the package posts and six aluminum wires bonded to devices and to the substrate gold metallization were pulled to destruction and the failure modes recorded. These pull tests, prior to coating, provided baseline bond strength data.

Table 2. Description of Silicone Coatings Selected for Evaluation

Coating Designation	Percent Solids	Viscosity Centistokes	Film Description
E2907-43-1	27.1	49	Clear, waxy, does not melt or flow below 150°C, flows under pressure at 85°C, dimethylpolysiloxane type
E2907-44-1	25.5	506	Clear, hard, tough coating, melting point 285-289°C, block copolymer of α-methylstyrene and dimethylpolysiloxane
E2907-47-1	16.0	570	Clear, tacky, flows under pressure at room temperature, dimethylpolysiloxane type.

Table 3. Description of Halocarbon Waxes Selected for Evaluation

Serial No.	Melting Point or Pour Point	Solubility
6-00	60°C	Freon TF, Toluene
12-00	120°C	Freon TF, Toluene
15-00	144°C	Toluene
19-00	210-220°C	Insoluble

In the remaining packages (which did not have a minimum of 12 gold wire post bonds or a minimum of 12 aluminum device-substrate bonds), half of each wire-bond type was destructively pull-tested and the failure modes recorded.

After some experience was gained in coating about 30 reject circuits, 32 circuits were coated for testing. Eight circuits were coated with each of the three silicones and eight were coated with a 1:1 mixture of DC-E2907-44-1 with Halocarbon 15-00. Not all of the solid Halocarbon 15-00 was soluble in xylene so only the xylene soluble portion (97.6%) was utilized in the mixed coating formulation. The three as-received silicones were further diluted with xylene to give solutions ranging from 6.4 to 10.8% solids as shown in Table 4.

3.1.1.2 Cleaning of Circuits

The circuits were cleaned by immersion in toluene for 30 to 60 seconds, followed by rinses in toluene, isopropyl alcohol, and Freon TF. The circuits were then air dried and inspected at 30X magnification for cleanliness. Circuits with visible loose particles were re-cleaned.

3.1.1.3 Application of Coating

The coating was applied with a dropping pipette (medicine dropper) while the microcircuit assembly was held under a microscope. Coating levels were examined during application to insure that all devices, wire bonds, and package posts were submerged in the coating. The coating was then poured out of the packages and the packages were inverted for 10 to 15 minutes to drain. Only the leads to the 42-lead wire bond test packages were masked during coating. The packages were then placed in upright positions and air-dried overnight.

3.1.1.4 Drying of Coating

The coated circuits were baked for one hour in nitrogen at 150°C $\pm$ 10°C to remove the solvent then vacuum baked four hours at 135 $\pm$ 10°C at less than one Torr pressure. The vacuum bake exposure was chosen to simulate conditions that the circuits are exposed to prior to hermetic sealing.

TABLE 4. CONCENTRATION OF APPLIED COATINGS

Silicone Coating	As Received	As Applied
E-2907-43-1	27.1% solids in toluene	10.8% solids in toluene and xylene
E-2907-44-1	25.5% solids in toluene	6.4% solids in toluene and xylene
E-2907-47-1	16.0% solids in toluene	6.4% solids in toluene and xylene

3.1.1.5 Coating Coverage

The coated hybrid circuits were examined at 7 to 30X magnification (before and after vacuum bake) to assure coating coverage of wires, devices, package posts, and substrates. The coatings could be seen on the substrates, package posts, and on all devices other than on the top of most rectangular ceramic chip capacitors. These capacitors may require additional coating (i.e.; touch up). However, it has not been determined whether the coating was adsorbed and/or absorbed on the capacitor surface or whether the coatings did not wet this particular device. Because of the transparency of the coatings, it could not be visually verified whether all the wires were completely coated. Aluminum wires (in close proximity on the same devices) and gold wires with both ends bonded to the substrate (jumpers) were bridged by the coatings, even after vacuum bake. In general, the coatings applied in these particular concentrations were thicker around the base of the devices.

3.1.1.6 Coating Removal Procedure

The three coatings were initially stripped from half of the circuits with Freon TF at 45.3 $\pm$ 2.3°C using a laboratory Soxhlet extractor. The minimum times required to remove the coatings were not established in this initial work. The Soxhlet stripping, however, consisted of nine cycles or about 1.5 hours. Silicones E2907-43-1 and 47-1 left a glossy residue on the substrates after the Freon TF stripping cycles. All three groups of stripped assemblies were soaked in isopropyl alcohol for two hours at ambient. They were then rinsed with fresh

isopropyl alcohol and then with fresh Freon TF. There were still minor traces of residues on the substrates that had been coated with E2907-43-1 and E2907-47-1 (later work established that these residues were not from the coatings). All circuits were then used for the rebond evaluations of gold and aluminum wires.

3.1.1.7 Wire Bond Pull Test Results

Aluminum and gold wires were rebonded (ultrasonically) and then destructively tested. The results of the rebond data were compared with the rebond data for a control group where no coatings were used and with the original bond data for each hybrid assembly. The bond and rebond data are summarized in Tables 5 and 6. The rebond and bond strength data clearly show that there were no differences between the strengths of aluminum and gold wire bonds made before and after coating removal. In fact, an improvement in bond strength seems to have occurred in some cases. This may be explained by a deterioration of bond strength for the initial bonds because of aging (up to 10 years in the case of some circuits) versus the higher strength for the newly formed bonds.

3.2 CHARACTERIZATION OF COATING MATERIALS (PHASE II)

The silicone and fluorocarbon materials were characterized by measuring their chemical, thermal and electrical properties and comparing them with several established semiconductor junction coatings. Results of these evaluations are given in the following sections:

3.2.1 Chemical Characterization

The Dow Corning silicones DC-E2907-43-1 and DC-E2907-47-1 are reported to be linear polydimethylsiloxane, while the third silicone DC-E2907-44-1 is a block copolymer of α-methylstyrene and polydimethylsiloxane. Molecular structures for these silicones are given in Figures 5 and 6. The halocarbon waxes are low-to-medium molecular weight polymers of chlorotrifluoroethylene which have been separated by vacuum distillation into various molecular weight fractions. A generic molecular structure is given in Figure 7. These coatings were characterized chemically by performing the following analyses:

- Infrared spectroscopy
- Atomic absorption spectroscopy for sodium and potassium ions
- Emission spectroscopy for all metal ions
- Titration for chloride ions
- Molecular weight determination by gel permeation chromatography

TABLE 5. EFFECT OF COATING REWORK ON ONE-MIL ALUMINUM ULTRASONIC BONDS

COATING	CONDITION	MEAN BOND* STRENGTH (GMS)	STANDARD DEVIATION	REMARKS
DC-E2907-43-1	BEFORE COATING	5.7	2.64	ORIGINAL US BONDS
	COATING REMOVED	7.4	1.27	ORIGINAL US BONDS
	REWORK BONDS	8.5	1.56	NEW US BONDS
DC-E2907-44-1	BEFORE COATING	5.6	2.08	ORIGINAL US BONDS
	COATING REMOVED	7.7	1.91	ORIGINAL US BONDS
	REWORK BONDS	8.6	1.89	NEW US BONDS
DC-E2907-47-1	BEFORE COATING	7.2	2.90	ORIGINAL US BONDS
	COATING REMOVED	8.9	2.04	ORIGINAL US BONDS
	REWORK BONDS	8.0	1.80	NEW US BONDS
CONTROL	REWORK BONDS	7.0	2.33	NEW US BONDS

* ALL BONDS FROM DEVICE THIN-FILM ALUMINUM METALLIZATION TO SUBSTRATE THIN-FILM GOLD METALLIZATION. MEAN OF 15 TO 24 BONDS ON FOUR REJECT HYBRID CIRCUITS FOR COATED SPECIMENS AND 10 BONDS ON ONE REJECT HYBRID CIRCUIT FOR CONTROL.

TABLE 6. EFFECT OF COATING REWORK ON TWO-MIL GOLD THERMOCOMPRESSION BONDS

COATING	CONDITION	MEAN BOND* STRENGTH (GMS)	STANDARD DEVIATION	REMARKS
DC-E2907-43-1	BEFORE COATING	23.3	5.75	ORIGINAL TC BONDS
	COATING REMOVED	23.8	6.03	ORIGINAL TC BONDS
	REWORK BONDS	26.1	5.67	NEW TC BONDS
DC-E2907-44-1	BEFORE COATING	22.8	3.73	ORIGINAL TC BONDS
	COATING REMOVED	23.9	3.26	ORIGINAL TC BONDS
	REWORK BONDS	21.8	3.30	NEW TC BONDS
DC-E2907-47-1	BEFORE COATING	22.0	4.74	ORIGINAL TC BONDS
	COATING REMOVED	24.8	6.50	ORIGINAL TC BONDS
	REWORK BONDS	24.2	5.26	NEW TC BONDS
CONTROL	REWORK BONDS	24.5	2.15	NEW TC BONDS

* ALL BONDS FROM SUBSTRATE THIN FILM GOLD METALLIZATION TO PACKAGE LEADS. MEAN OF 18 TO 24 BONDS ON FOUR REJECT HYBRID CIRCUITS FOR COATED SPECIMENS AND 10 BONDS ON ONE REJECT HYBRID CIRCUIT FOR CONTROL.

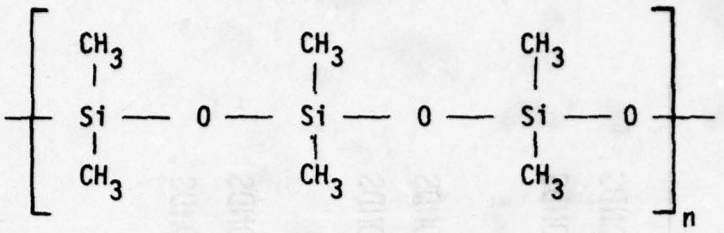


Figure 5. Molecular Structure for Linear Polydimethylsiloxane

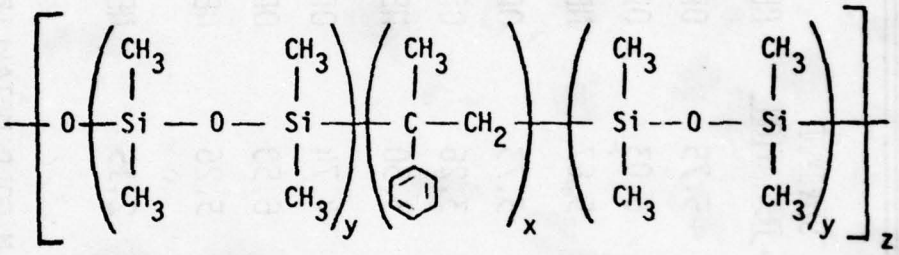


Figure 6. Molecular Structure for Block Co-Polymer of α-methylstyrene and Polydimethylsiloxane

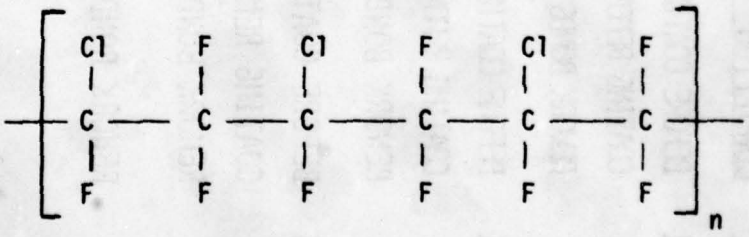


Figure 7. Molecular Structure for Polychlorotrifluoroethylene

3.2.1.1 Infrared Absorption Spectroscopy

The infrared (IR) absorption spectra in the region of 2.5 μm to 40 μm were obtained for each of the coating materials. Infrared spectra are important as indicators of chemical composition and molecular structure as well as reference standards for assuring quality control of subsequent batches. The IR spectra for the three silicones were obtained after removal of the toluene solvent by evaporation. Spectra for these silicones are given in Figures 8, 9 and 10.

Infrared spectra were also obtained for the halocarbon waxes (as received in the solid form) for types 12-00, 15-00, and 19-00. Type 19-00 was received as a powder and is normally used by Halocarbon Products Corp. as a thickener for some of their greases. Type 19-00 is not a likely candidate for this study because it is not soluble in Freon TF or toluene. The infrared spectra are shown in Figures 11, 12 and 13.

Type 15-00 wax is partially formulated by adding type 19-00 dissolved in Type 8-00 wax. Type 8-00 wax has a melting point or pour point of 81.1°C.

The sample labeled as 12-00 showed the presence of contamination as evidenced by infrared absorption bands at wave numbers 3300, 2920, 2250, 1700, 1600, 1550, and 1400 cm^{-1}. When the IR spectrum was re-run using a sample from within the bulk of the 12-00 wax, the spectrum did not show contaminants and it was therefore concluded that contamination in the original samples had been introduced during handling and sampling (Figure 14).

3.2.1.2 Analyses for Ionic and Metal Impurities

Sodium and potassium ions in low parts-per-million concentrations are known to cause inversion currents and increased leakage currents, and to affect the beta value of active semiconductor devices. Minimizing the concentration of these deleterious ions on circuits having semiconductor devices is therefore important. Other metal impurities are also critical and can contribute to surface leakage currents and to corrosion of thin-film metallization. Chloride ions on hybrid microcircuit surfaces are also deleterious from a corrosion and leakage current standpoint.

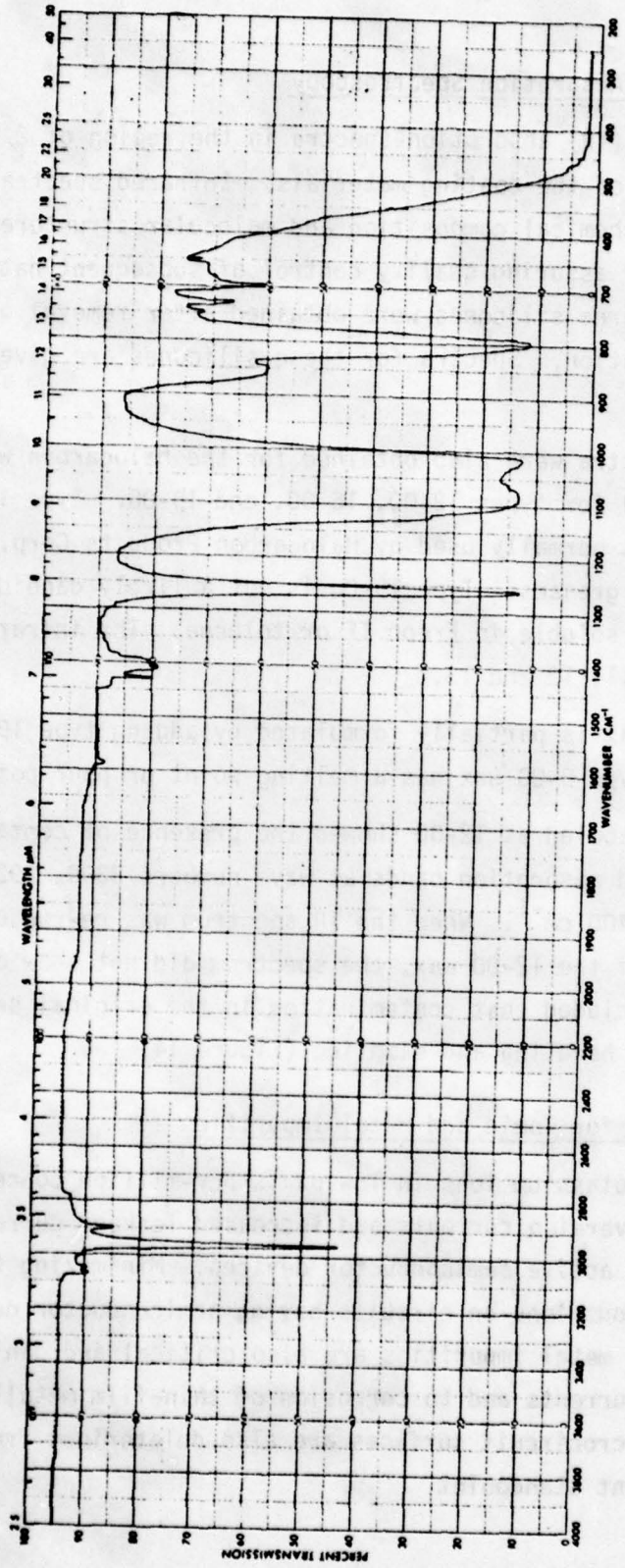


Figure 8. Infrared Spectrum of Solvent Free Silicone Coating - E2907-43-1

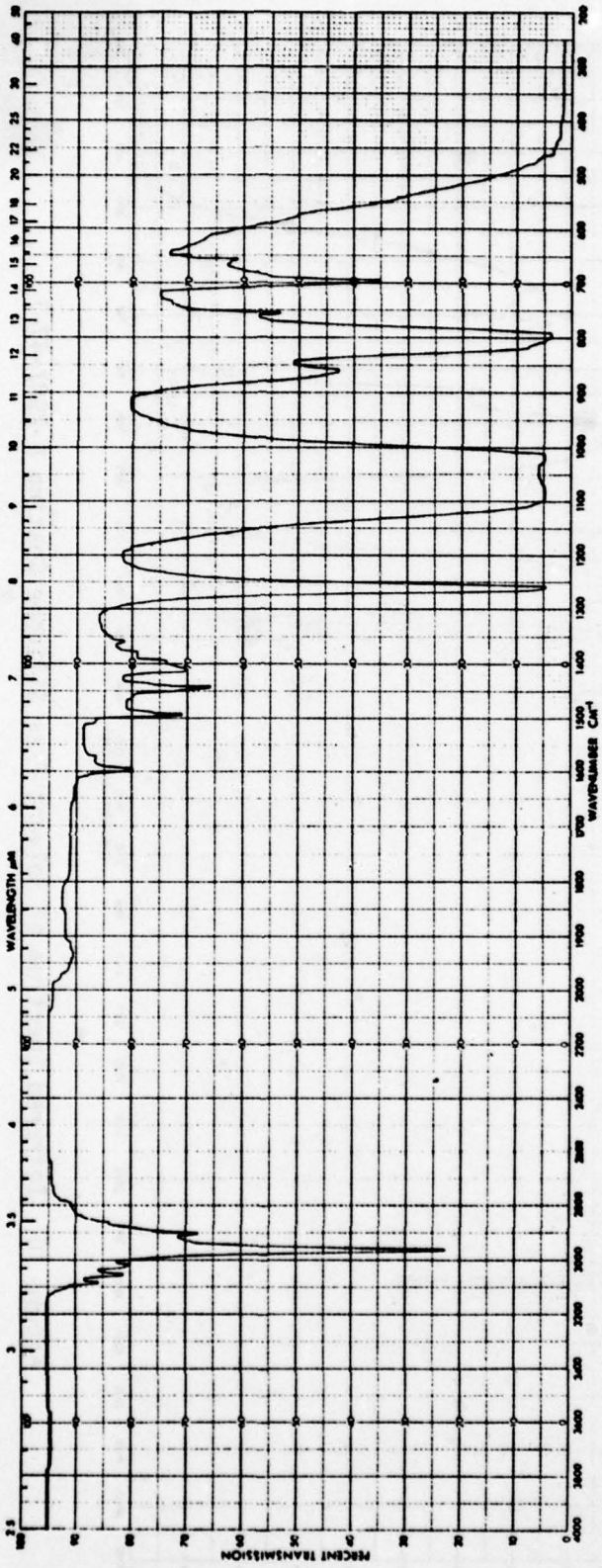


Figure 9. Infrared Spectrum of Solvent Free Silicone Coating - E-2907-44-1

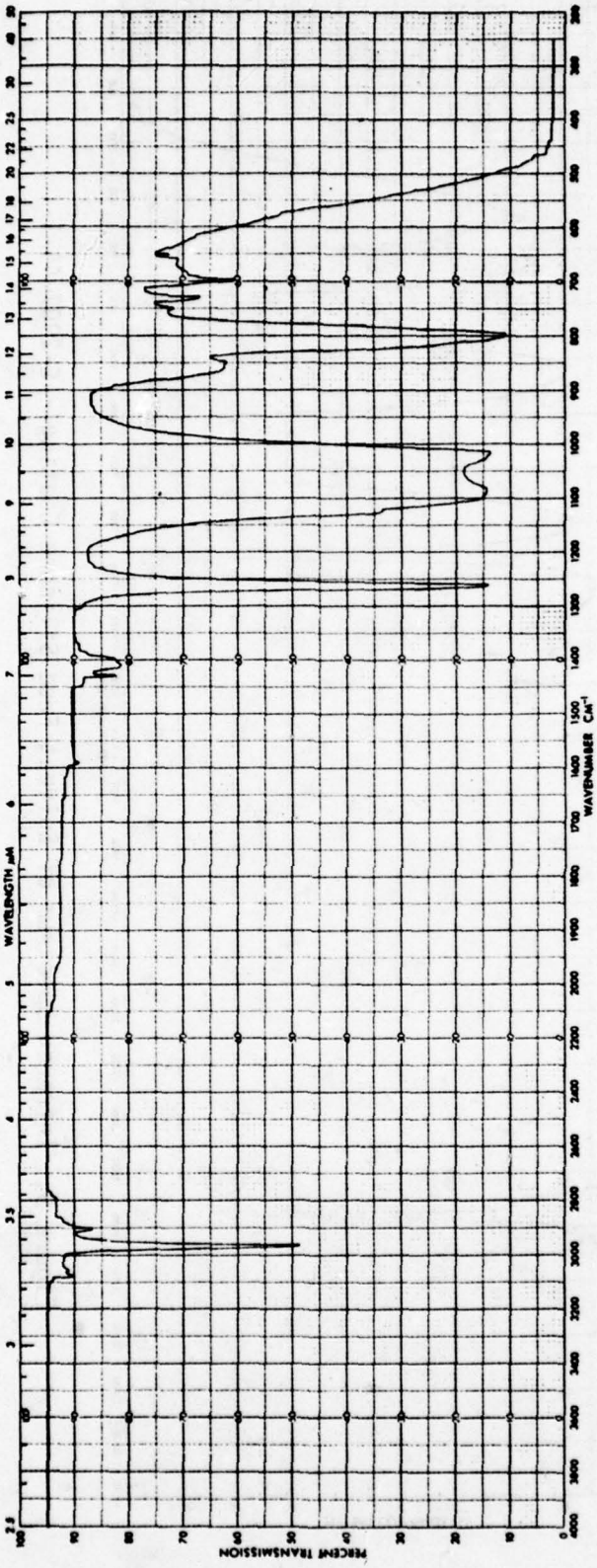


Figure 10. Infrared Spectrum of Solvent Free Silicone Coating E-2907-47-1

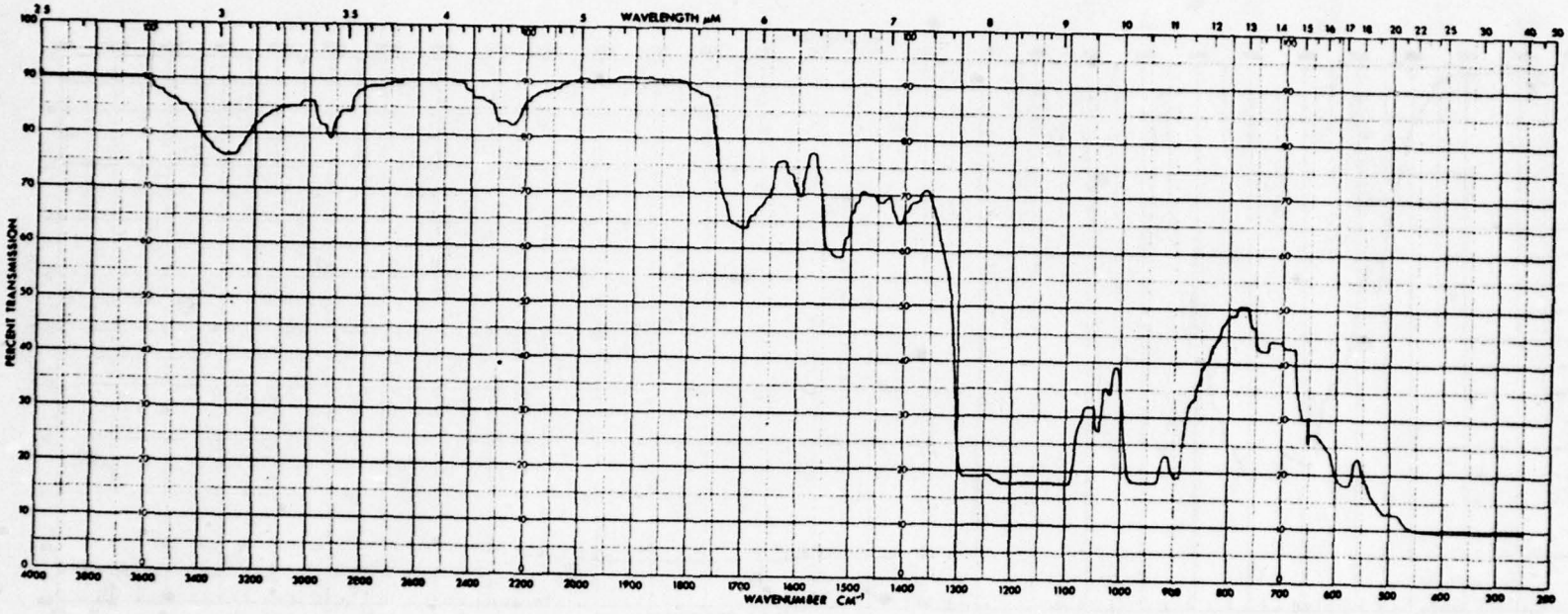


Figure 11. Infrared Spectrum of Halocarbon Wax, Type 12-00, Showing the Presence of Contamination Introduced During Sampling

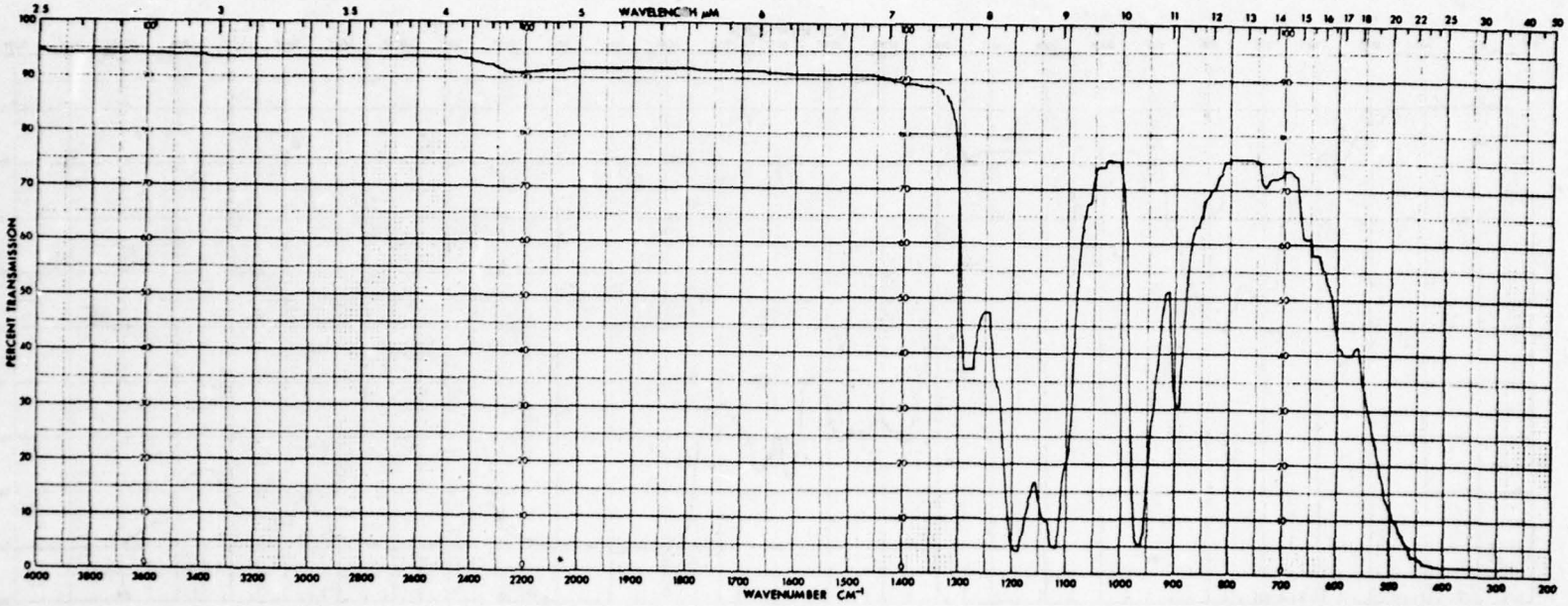


Figure 12. Infrared Spectrum of Halocarbon Wax, Type 15-00

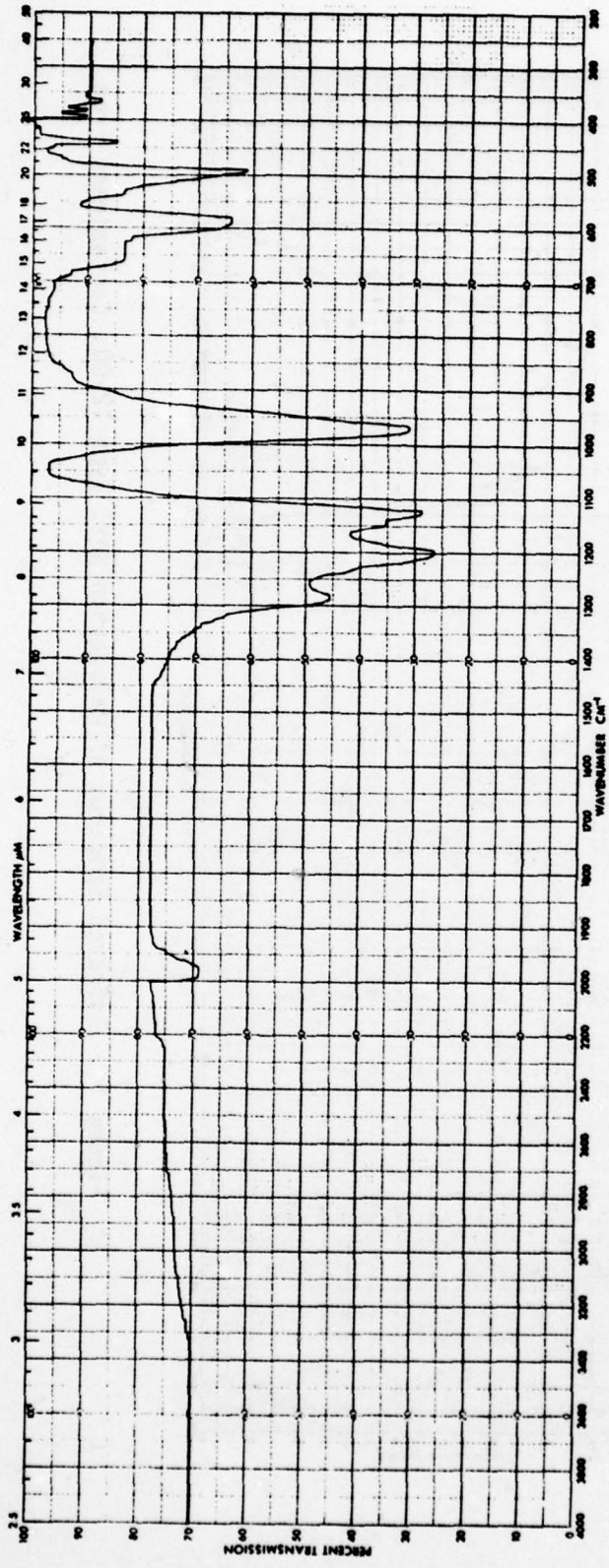


Figure 13. Infrared Spectrum of Halocarbon Wax, Type 19-00

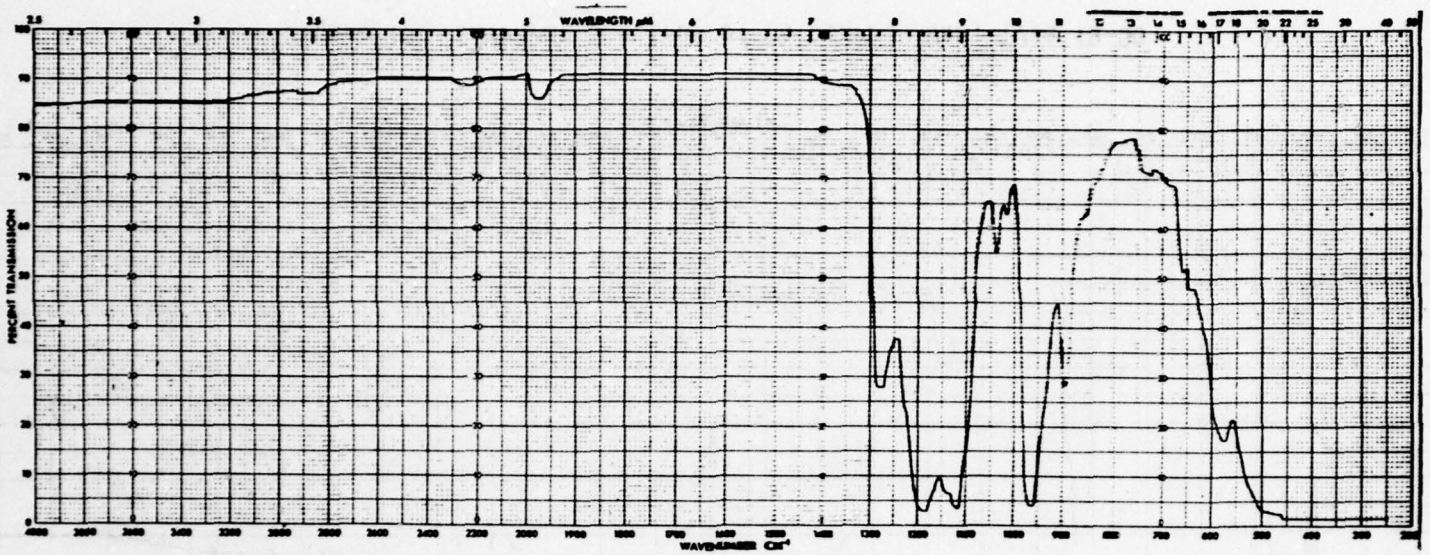


Figure 14. Infrared Spectrum of Halocarbon Wax, Type 12-00, Contaminant Free

The three silicone coatings, two halocarbon coatings, and a fluoroescent dye (Shannon C-007) were analyzed for sodium and potassium ions (by atomic absorption spectroscopy); for other metal impurities (by emission spectroscopy); and for chloride ions (by mercuric nitrate titration). Analyses were performed by West Coast Technical Services, Cerritos, CA and their results are reported in Table 7. The fluoroescent dye was a recommendation of Dow Corning to be used as an additive to the coatings to facilitate visual inspection of coating coverage on the circuit. Sodium ion concentrations for the coatings ranged from 33 to 60 ppm by weight and potassium ion concentrations ranged from about 8 to 18 ppm by weight. However, sodium levels reported by Dow Corning are all less than 1 ppm. Though the sodium and potassium ion levels were found to be higher than reported, they may still not be critical to the hybrid circuit performance. To establish this, a study of the effects of the coating on a variety of contaminant sensitive semiconductor devices was performed (see Section 3.2.3). Other firms who have analyzed silicone materials have encountered similar discrepancies (reference 3). These discrepancies require further investigation but could not be accommodated under this contract.

3.2.1.3 Molecular Weights by Gel Permeation Chromatography (GPC)

Gel permeation chromatography involves flowing a sample of the polymer dissolved in a compatible organic solvent through a column that is packed with a rigid highly porous gel. Separation of the individual molecules or molecular weight fragments occurs along the column because of differences in physical adsorption and absorption in the gel. The smaller molecular weight fractions permeate the gel pores more easily and therefore take extra time to reach the bottom. The higher molecular weight fractions, however, will emerge sooner from the column. A GPC detector monitors the passage of the different sized molecules and measures their concentrations. The information is recorded on a strip chart in the form of molecular weight distributions (reference 4). The molecular weight distribution of a polymer is an important characteristic which influences properties such as flow, reactivity, outgassing, and hardness. Subtle batch-to-batch variations which may cause significant differences in end use performance can be detected making GPC a good quality control and receiving inspection test.

TABLE 7. CHEMICAL ANALYSES OF COATING MATERIALS AFTER SOLVENT REMOVAL

Method/Element	DC E2907-43-1	DC E2907-44-1	DC E2907-47-1	Halocarbon 12-00	Halocarbon 15-00	Shannon C-007
Emission/Spectroscopy						
Silicon	27 wt. %	24 wt. %	24 wt. %	460 ppm W/W	390 ppm W/W	150 ppm W/W
Magnesium	0.00078	0.00022	0.00015	2.2	1.1	1.2
Iron	ND<0.0009	0.0023	0.0020	20	11	9.3
Boron	ND<0.005	ND<0.005	ND<0.005	1.3	0.17	ND <0.30
Aluminum	ND<0.0003	0.00083	ND<0.0003	10	5.1	4.2
Copper	0.000035	0.00010	0.000032	0.70	0.33	1.6
Silver	ND<0.00005	TR<0.0005	ND<0.00005	ND<0.10	TR<0.10	0.088
Sodium	ND<0.02	ND<0.02	ND<0.02	ND<50	TR<50	83
Titanium	0.0017	ND<0.0005	ND<0.0005	ND<1.0	ND<1.0	TR<0.30
Nickel	ND<0.0003	TR<0.0003	ND<0.0003	ND<1.0	ND<1.0	4.6
Strontium	ND<0.001	ND<0.001	ND<0.001	ND<1.0	ND<1.0	TR<0.20
Calcium	0.00043	0.00069	0.00046	4.2	2.7	1.8
Loss on ignition	41.72	48.86	48.12	99.8896	99.9198	99.9351
Atomic Absorption						
Sodium	44.3 ppm W/W	60.4 ppm W/W	33.3 ppm W/W	47.8 ppm W/W	54.3 ppm W/W	60.4 ppm W/W
Potassium	12.1 ppm W/W	18.5 ppm W/W	7.6 ppm W/W	14.3 ppm W/W	12.8 ppm W/W	24.7 ppm W/W
Titration						
Chloride	60 ppm W/W	209 ppm W/W	110 ppm W/W	153 ppm W/W	62 ppm W/W	240 ppm W/W
Vendor Data						
Sodium	<1.0 ppm W/W	<1.0 ppm W/W	<1.0 ppm W/W	-	-	-
Potassium	<1.0 ppm W/W	<1.0 ppm W/W	<1.0 ppm W/W	-	-	-

Molecular weights of two lots of DC-E2907-44-1 silicone, and one lot of Halocarbon 15-00 were determined using GPC analysis. The coatings were dissolved in tetrahydrofurane solvent and passed through columns of microstyragel. Both lots of the silicone had average molecular weights of 100,000 and the soluble portion of the halocarbon had an average molecular weight of 1100. Records of the determinations are given in Figures 15, 16 & 17.

GPC analysis on the two lots of DC-E2907-44-1 also showed reproducibility from lot to lot. Gel permeation chromatography therefore appears to be a good analytical tool not only for qualification of resin but also for receiving inspection.

Thermal Characterization

The thermal stability of the coatings was determined by thermogravimetric analysis (TGA). This method consists in accurately and dynamically measuring the weight loss using a Cahn electrobalance on which the sample is heated at a programmed temperature increase. The temperature at which outgassing of solvents and other low boiling constituents and the temperature at which complete decomposition of the molecules occurs may be obtained from the TGA curves. The TGAs were performed in a nitrogen environment using a Perkin-Elmer TGS-1 equipment at a temperature rise of 10°C per minute.

TGA curves were run for the three silicone coatings and for two of the halocarbon samples. The initial set of analyses was performed on silicone samples after the solvent had been evaporated and the residue had been baked at 150°C for 30 minutes. The halocarbon was analyzed on "as-received" samples because it was a solid wax. Curves obtained are given in Figures 18 and 19.

A second set of TGA curves was run on samples that had been vacuum baked according to conditions normally used in production prior to hermetically sealing the packages. These conditions are more representative of those encountered in a manufacturing line. This second set of samples was baked at 150°C for 30 minutes followed by 4 hours at 135°C under <1.0 Torr pressure. The TGA curves are given in Figures 20 and 21.

All coatings showed weight losses of less than 0.25 percent at 200°C after the vacuum bake. With the exception of silicone coating E2907-43-1,

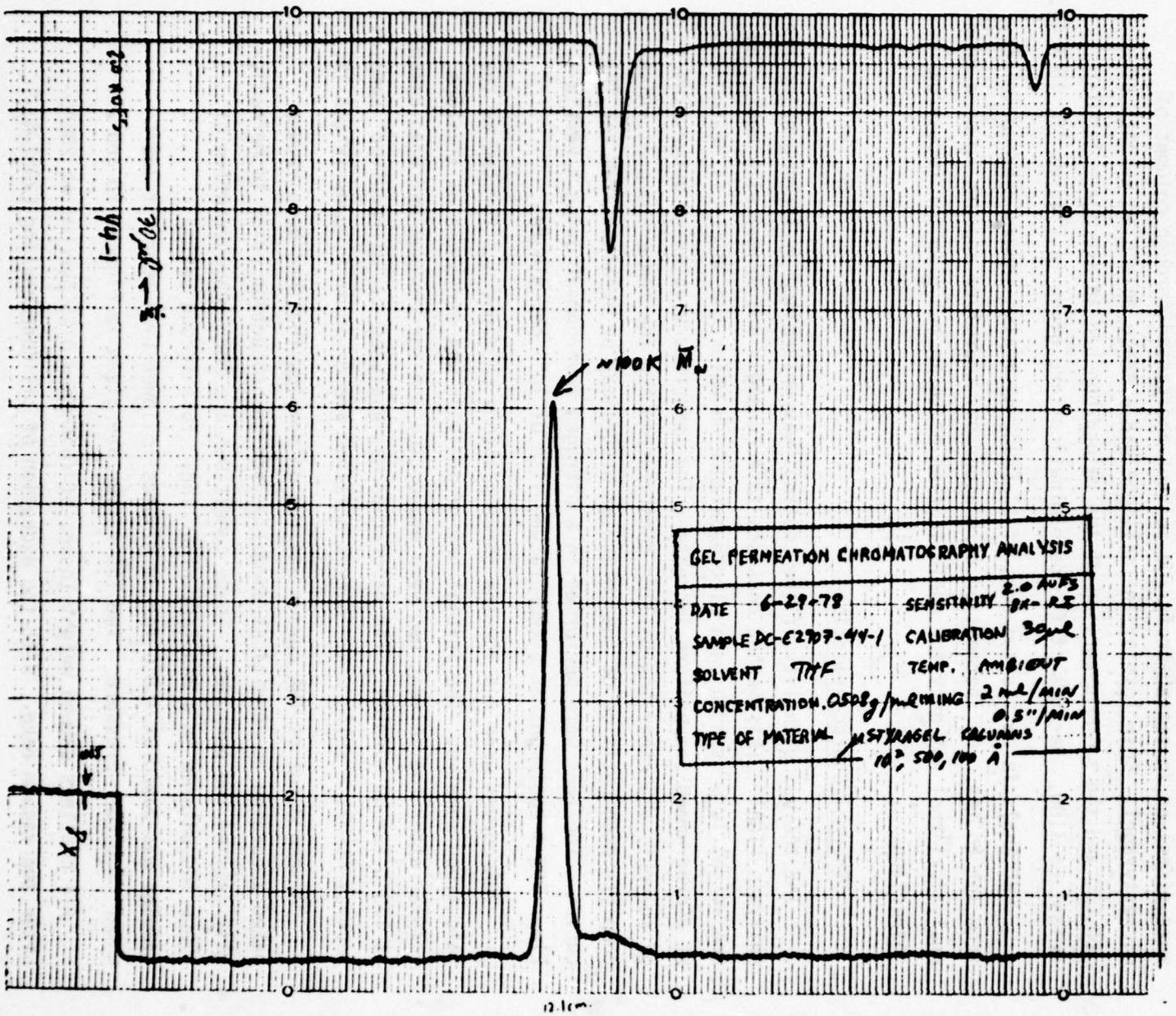


Figure 15. Molecular Weight Determination of DC-E2907-44-1 Silicone

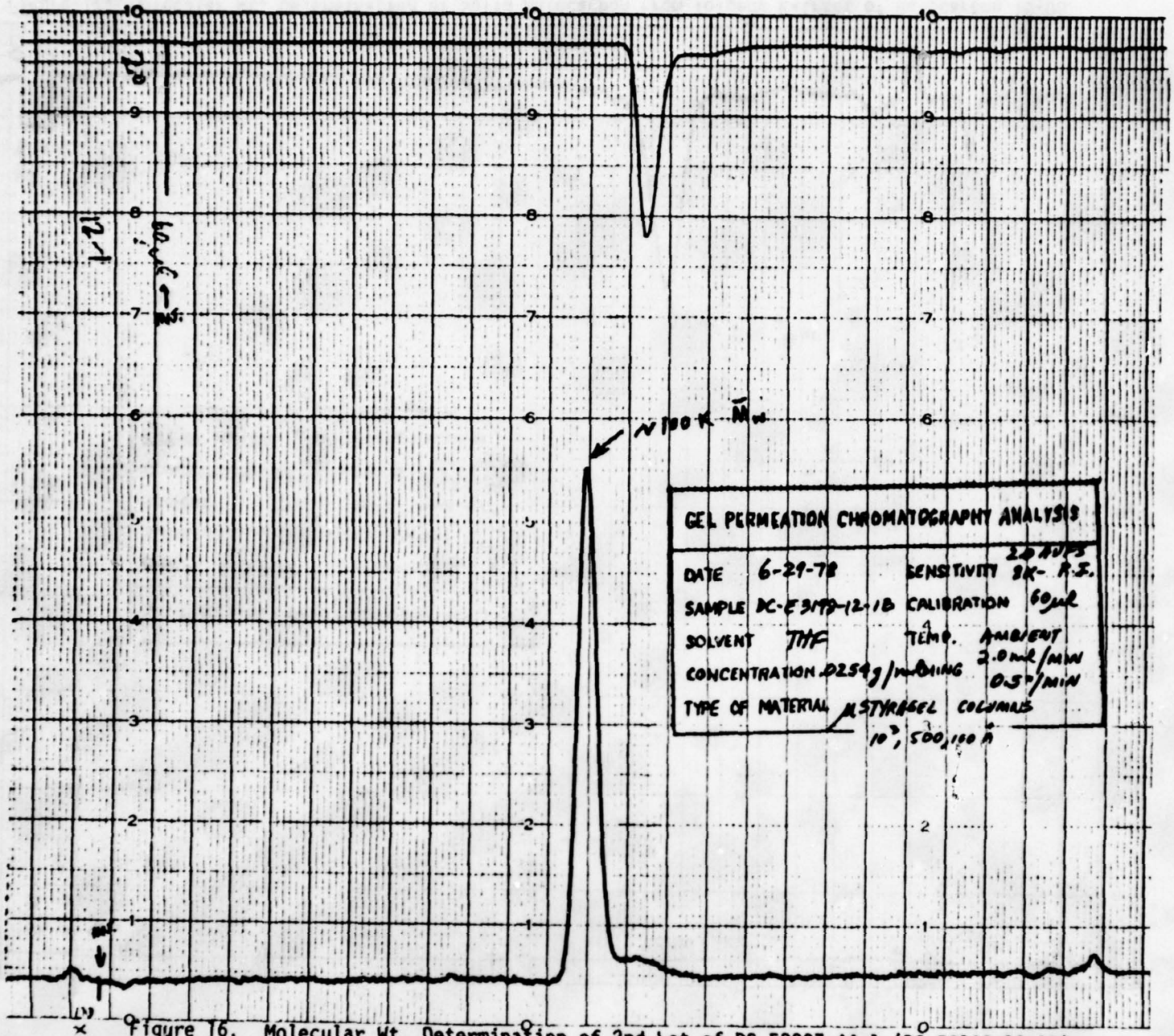


Figure 16. Molecular Wt. Determination of 2nd Lot of DC-E2907-44-1 (DC-E3198-12-1B)

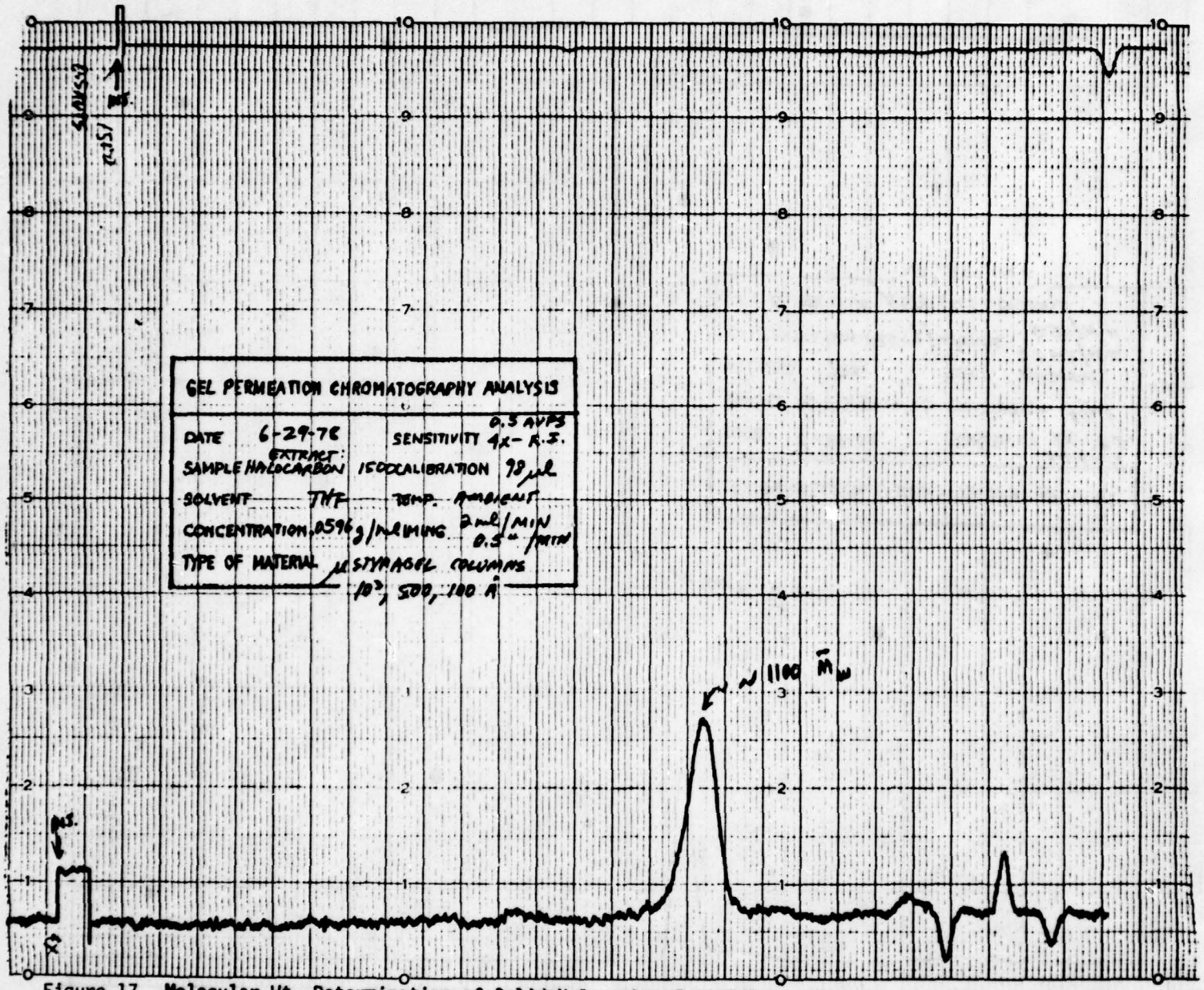


Figure 17. Molecular Wt. Determination of Solid Halocarbon From Toluene Extract of Halocarbon 15-00

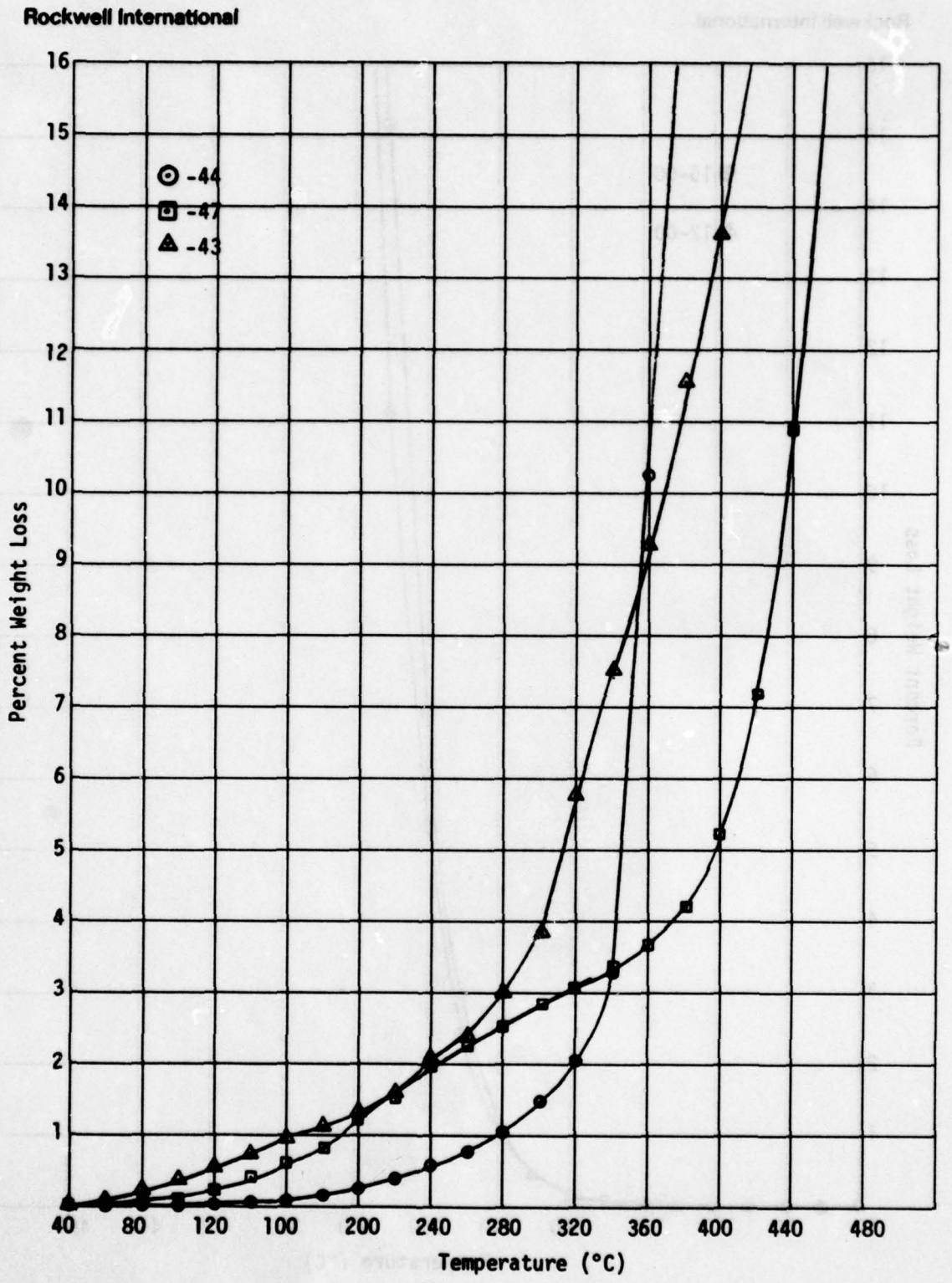


Figure 18. TGA Curves for Silicone Coatings Without Vacuum Bake-out

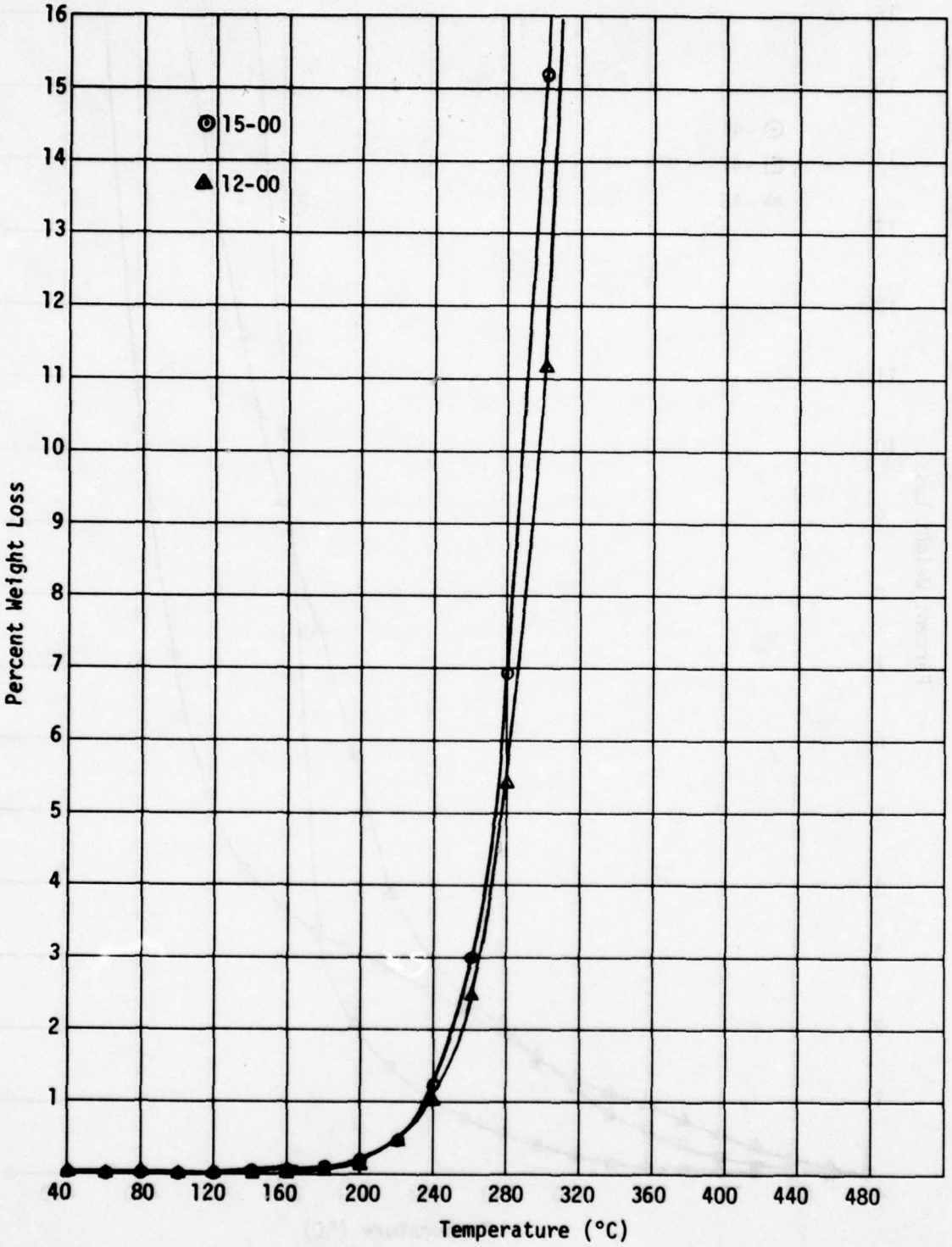


Figure 19. TGA Curves for Halocarbon Waxes 12-00 and 15-00 Without Vacuum Bake-out

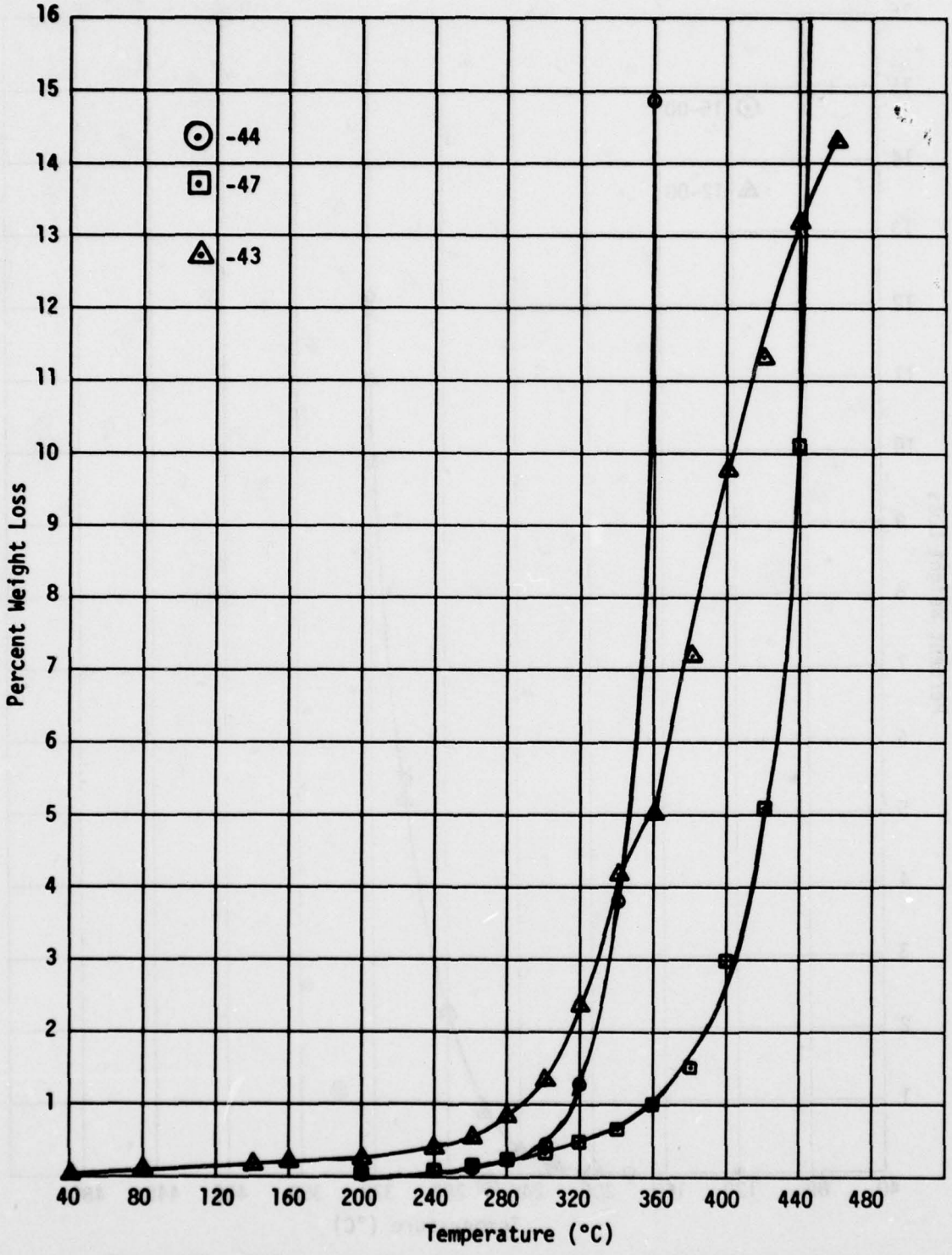


Figure 20. TGA Curves for Silicone Coatings After Vacuum Bake-Out for Four Hours at 135°C at <1.0 Torr Pressure

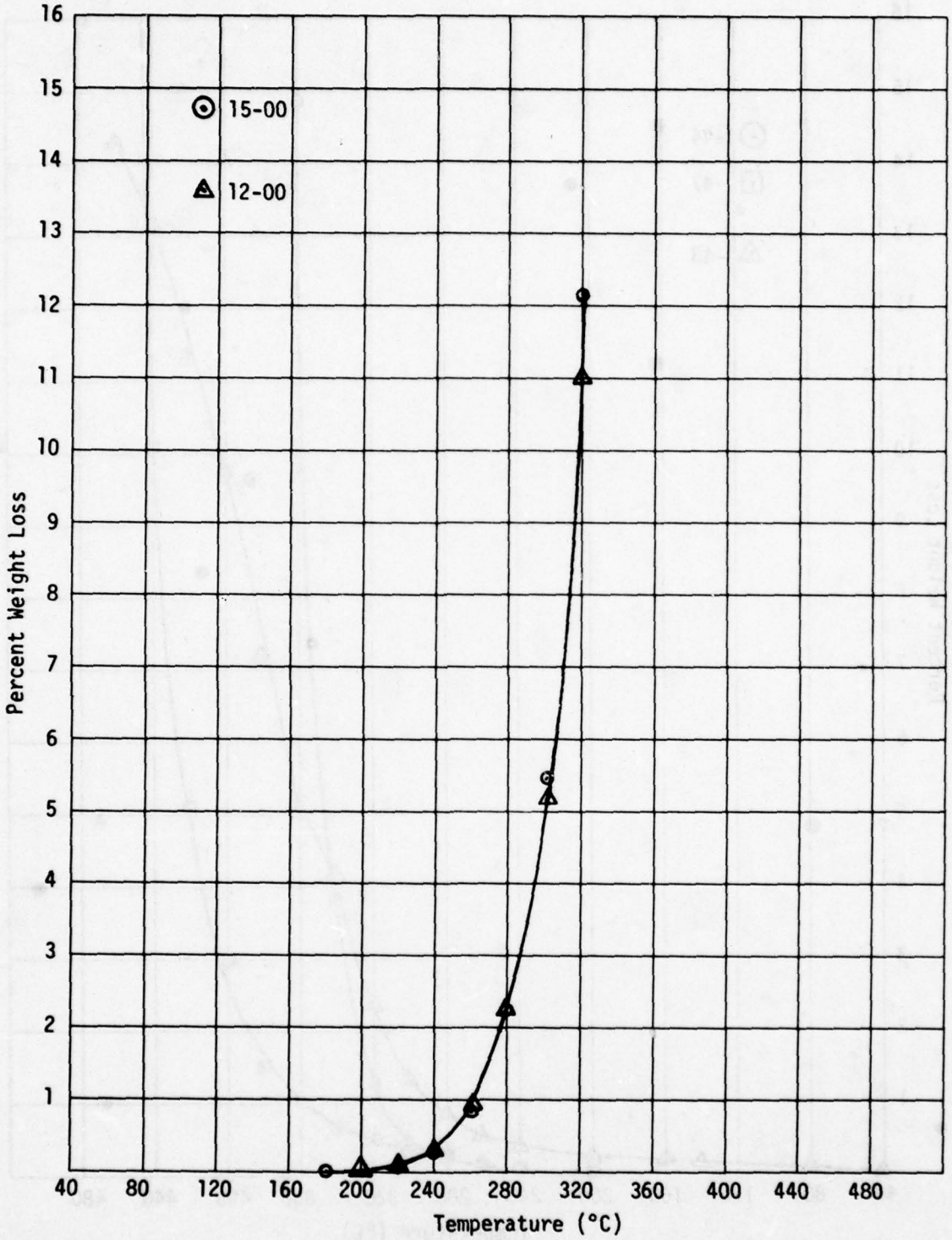


Figure 21. TGA Curves for Halocarbon Waxes After Vacuum Bake-Out for Four Hours at 135°C at <1.0 Torr Pressure

none of the coatings showed any weight loss below 180°C. The E2907-43-1 coating apparently contains a broader range of molecular weight fractions than the other two silicone coatings. The samples were exposed to room ambient after vacuum bake-out. The low temperature outgassing of E2907-43-1 indicated absorption of the ambient moisture during this exposure. As a result of these data, E2907-43-1 was dropped from further consideration.

3.2.3 Electrical Characterization

3.2.3.1 Coating Effects on P-MOS Devices

An evaluation of the electrical effects of each of the three silicone coatings was conducted on specially designed silicone wafers having closely spaced aluminum lines and on process evaluation chips having numerous P-MOS devices. Surface leakages and transistor threshold voltage and leakage measurements were made.

Silicon wafers three inches in diameter containing devices with thin film aluminum comb structures, as shown in Figure 22, were fabricated for the surface leakage measurements. Half of the wafers had silox over the aluminum pattern and the other half had no silox. The wafers were coated in the pattern shown in Figure 23. Each coating was applied to one wafer with silox and one without. Two of the comb circuits were measured for leakage in each of the quadrants shown in Figure 23. A Keithly 616 electrometer was used to measure the surface leakage current resulting from 20 volts applied to the comb structures which contained 0.3 mil lines and spaces. Each structure contains 27 lines, 63.0 mils in length for a total of 5,460 squares.

For the transistor threshold and leakage tests, two wafers containing Process Evaluation Chips (PECs), Figure 24., used to evaluate PMOS processes and their effect on device electrical behavior were used. The wafers were quartered and each of the three quarters of one wafer was dip coated with one of the silicone solutions and one quarter was left uncoated. Each of three quarters of the other wafer was spray coated with one of the silicone solutions and one quarter was left uncoated. The threshold voltages and the voltage at which one nanoamp of leakage current was observed were measured.

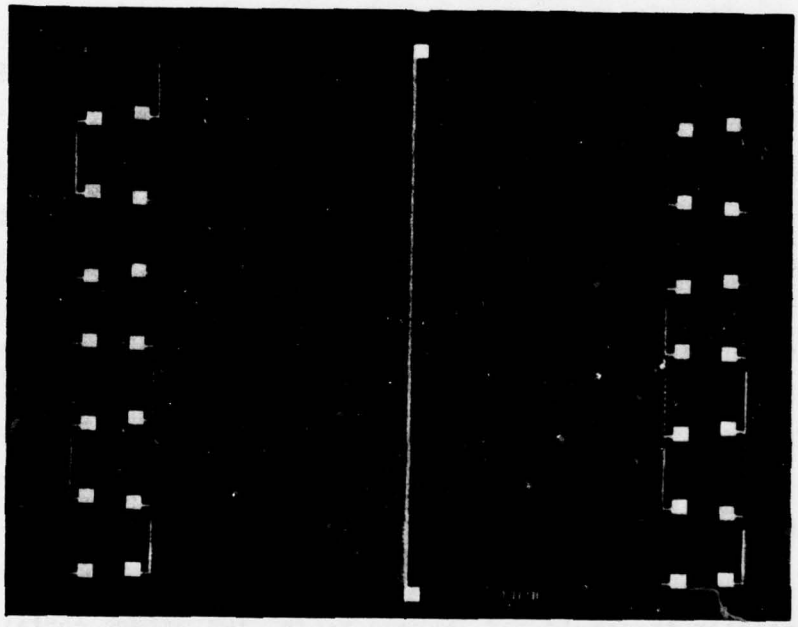


Figure 22. Comb Structure on Silicon Wafer Used for Surface Leakage Measurements

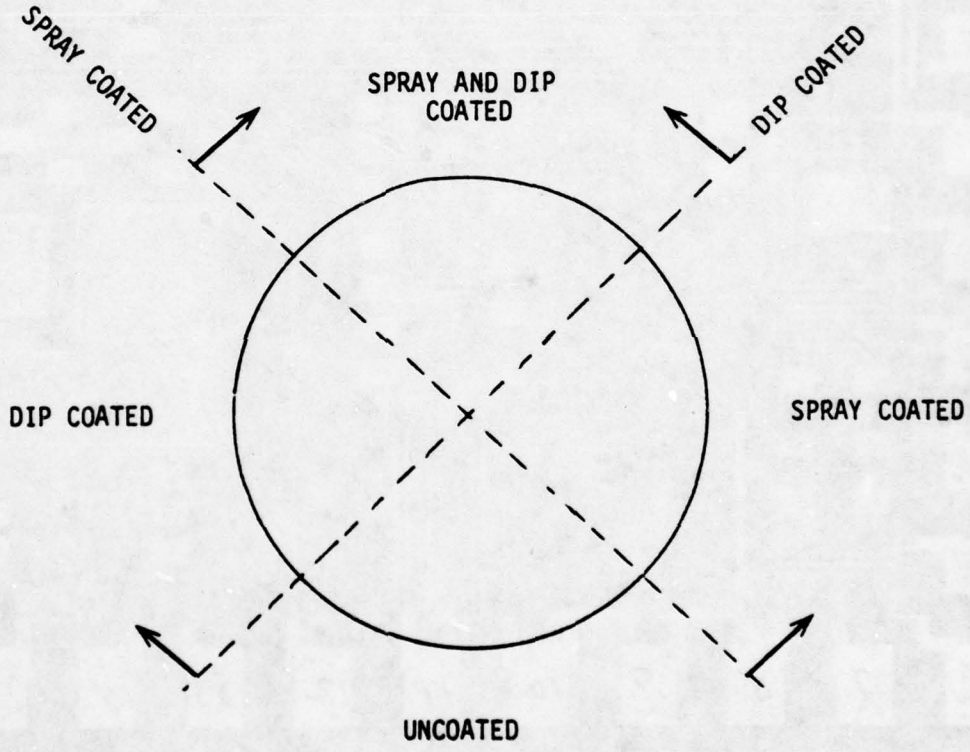


Figure 23. Wafer Coating Configuration

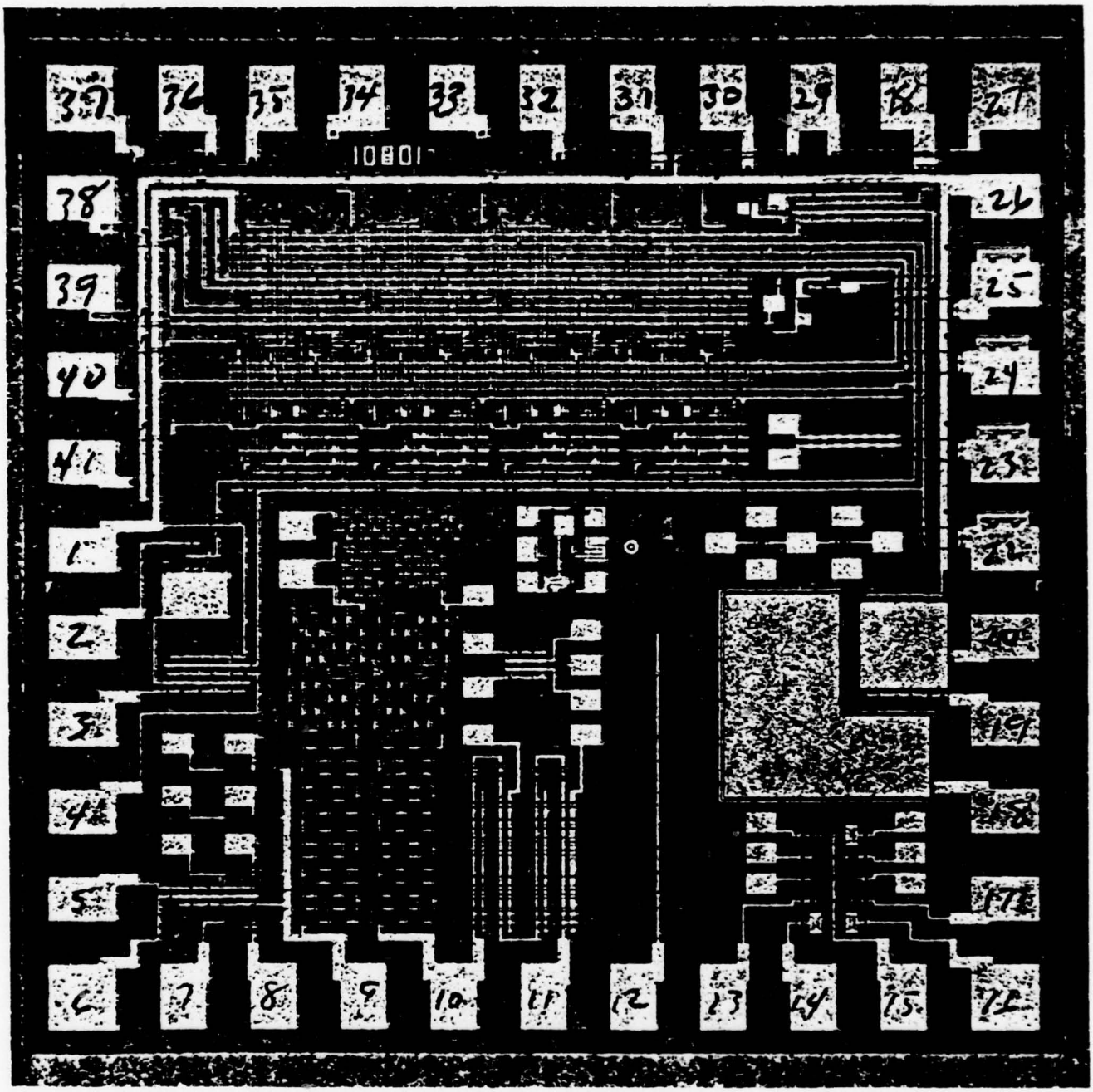


Figure 24. Process Evaluation Chip (PEC) Used for Measurement of Threshold Voltage and Leakage Changes

The results, tabulated in Table 8, indicate negligible surface leakage current and a surface resistivity similar to that of dry fused quartz for both the coated and uncoated comb structures. As shown in Table 9, the coatings also showed negligible effects on the threshold voltage and leakage of the PEC device.

3.2.3.2 Electrical Properties

Electrical properties that are important to the performance of a coating used as an insulation or dielectric include insulation resistance (volume resisitivity, surface resistance), dielectric strength, dielectric constant, and dissipation factor. Measurements of these electrical properties were made according to established ASTM and Military specifications as follows:

Test	Units	Procedure
Volume Resistivity	ohm-cm	ASTM D257-66
Insulation Resistance	ohm	MIL-STD-202
Dielectric Constant	-	ASTM D150-59T
Dissipation Factor	-	ASTM D150-59T
Dielectric Strength	volts/mil	ASTM-D149-59

Measurements were made at both 10^2 Hz and 10^5 Hz where possible. Electrical values for Dow Corning 6101, Dow Corning DC-90-711 and G.E. EJC-261, representative of state-of-the-art semiconductor junction coatings, are given for comparison (Table 10). The results (Table 10) show that the halocarbon waxes had electrical properties of the same order of magnitude, except for dielectric strength, as the DC-6101. The dielectric strengths were similar to those for Dow Corning fluorosilicone coatings (340-380 volts/mil) which are recommended for electrical insulation for connectors. It was difficult to prepare dimensionally accurate test samples for the DC-E2907-47-1 because of its inherent tackiness. Samples had to be prepared and measured several times. The somewhat lower dielectric strength and volume resistivity value may be attributed to these sample preparation problems. Generally, the electrical properties for the other coating materials were considered excellent and close to those of the best semiconductor junction and circuit coatings.

Table 8. Surface Leakage Currents and Surface Resistivity from Comb Structure

COATING TESTED	SILOX PRESENT	COATING APPLICATION		
Dow Corning E2907-43-1	No	None	Light Spray	2 Dips
		4.75×10^{-14} a 2.3×10^{18} Ω/□	4.75×10^{-14} a 2.3×10^{18} Ω/□	3.0×10^{-13} a 3.6×10^{17} Ω/□
	Yes	2.67×10^{-13} a 4.1×10^{17} Ω/□	3.0×10^{-13} a 3.6×10^{17} Ω/□	1.6×10^{-13} a 6.8×10^{17} Ω/□
Dow Corning E2907-44-1	No	None	Light Spray	1 Dip
		3.25×10^{-14} a 3.4×10^{18} Ω/□	3.88×10^{-14} a 2.8×10^{18} Ω/□	4.5×10^{-14} a 2.4×10^{18} Ω/□
	Yes	4.5×10^{-14} a 2.4×10^{18} Ω/□	5.38×10^{-14} a 2.0×10^{18} Ω/□	3.88×10^{-14} a 2.8×10^{18} Ω/□
Dow Corning E2907-47-1	No	None	Heavy Spray	1 Dip
		NO SAMPLES PREPARED		
	Yes	1.5×10^{-13} a 7.3×10^{17} Ω/□	1.63×10^{-13} a 6.7×10^{17} Ω/□	1.25×10^{-13} a 8.7×10^{17} Ω/□

Table 9. Threshold Voltages and Leakages Observed With Process Evaluation Chips

Coating	Method	Wafer	V_T	V_{os} @ 1 na
None		5 3	1.60V 1.54	23 V 28
E2907-43-1	Light Spray 2 Dips	5 3	1.43 1.55	25 24
E2907-44-1	Light Spray 1 Dip	5 3	1.45 1.57	25 27
E2907-47-1	Heavy Spray 1 Dip	5 3	1.55 1.54	25 24

TABLE 10. ELECTRICAL PROPERTIES OF COATING MATERIALS

MATERIAL	DIELECTRIC STRENGTH			VOL. RESISTIVITY (OHM-CM)		DIELECTRIC CONSTANT		DISSIPATION FACTOR	
	THICKNESS (MILS)	READING (VOLTS)	(VOLTS/MIL)	INITIAL	AFTER MOISTURE CONDITIONING	10^2 Hz	10^5 Hz	10^2 Hz	10^5 Hz
DC E2907-43-1	105	40,725	388	1.2×10^{16}	4.4×10^{15}*	3.23	3.12	0.005	0.000023
DC E2907-44-1	105	46,170	469	1.4×10^{16}	2.0×10^{15}*	2.62	2.64	0.0016	0.000036
DC E2907-47-1	115	26,180	228	5.1×10^{13}	1.9×10^{13}*	2.93	-	0.023	-
HALOCARBON 12-00	121	38,830	321	2.6×10^{15}	1.9×10^{15}**	3.76	3.11	0.016	0.0096
HALOCARBON 15-00	103	33,500	325	2.8×10^{15}	1.8×10^{15}**	3.39	3.05	0.0069	0.0064
DC5101	-	-	575	2.0×10^{15}	-	3.01	-	0.001	-
DC90-711	-	-	575	1.0×10^{14}	-	-	2.7	-	0.0004
GE EJC-261	-	-	480	1.8×10^{15}	-	-	2.83	-	0.001

* 10 DAYS AT 70°C AND 98% RH

** 10 DAYS AT 23°C AND 96% RH

3.2.4 Wire Bond Stress Evaluation

One of the most sensitive portions of a hybrid circuit, and one which has militated against the use of coatings in the past, are the fine wire bonds. Heavy coatings or coating bridging wires cause thin aluminum or gold wire (1-3 mils diameter) to break or bonds to lift because of their high expansion coefficients. A study of the effects of the coating on the reliability of wire bonds was therefore an important and critical portion of this program.

3.2.4.1 Wire Bond Test Samples

To conduct the bond stress evaluation, sixty (60) aluminum metallized (16,000 Å) silicon die (200 x 200 mils) were attached to 42-lead ceramic circuit packages (Autonetics IID 192-0311) with Eccobond 104 epoxy nonconductive adhesive. All 42 package leads in each package were ultrasonically bonded to the aluminum die metallization using 1.0 mil diameter gold wire. Each package therefore had 42 wire connections or 84 wire bonds. Six wires (12 wire bonds) for each package were destructively pull tested to provide a baseline with which to compare the subsequent effects of coating, temperature cycling, and moisture exposure. The total number of bonds that were evaluated for each coating was therefore 576 (72 bonds/package x 8 packages). Prior to testing, all wires were nondestructively pull tested at 2 grams. Coating effects on wire bonds were determined by changes in electrical resistance measurements of the bonds after temperature cycling and by changes in the mean value for bond strength.

3.2.4.2 Electrical Test Equipment

The equipment for the electrical resistance measurements consisted of a test connecting fixture for the 42-lead packages, a printed wiring board on which the connecting fixture had been soldered, and wires soldered onto the 42 circuit pads on the PWB to "banana-type" jacks. The electrical resistance of each pair of wire bonds (plus metallization path) was then measured on a calibrated digital ohmmeter. The baseline resistance measurements for this test equipment were determined by measuring the resistances of the test circuit which contained a 42-lead package with the leads shorted. Each jack was numbered to correspond to each package lead. Readings were repeatable

and the test equipment could be utilized for any measurement on any chosen pair of leads for this 42-lead package. A photograph of this test equipment is given in Figure 25.

3.2.4.3 Formulation of Coatings and Sample Preparation

Eight packages were flow coated with each of the three silicones (24 packages) but those coated with E2907-43-1 were not processed further because of the high outgassing noted earlier. Instead, these eight packages were stripped of their coating and reprocessed with one of the other coating combinations. An additional 10 packages were spray coated: Eight with the E2907-44-1 coating and two with the E2907-47-1 coating. Another 24 packages (8 per coating) were spray coated with mixtures of E2907-44-1 and toluene extract from Halocarbon 15-00 in 1:1, 2:1, and 3:1 ratios, respectively. Eight packages were left uncoated and used as controls. The E2907-44-1 and Halocarbon 15-00 were selected as the two best candidates to formulate in a mixed coating because they possessed the best combination of physical, thermal, and electrical properties. The mixed coatings were formulated as follows: Five grams of Halocarbon 15-00 were dissolved in 50 ml of xylene and the solution filtered to remove the high molecular weight insoluble fraction (about 2.4%). The solution was then further diluted with xylene to form a 6.4% (by weight) solution. Equal volumes of this solution and a 6.4% (by weight) solution of silicone E2907-44-1 in toluene and xylene were combined, poured into an aluminum cup, air dried overnight and baked at 150°C for one-half hour. While quantitative measurements were not made, the coating formulation showed excellent peel strength to the aluminum along with excellent tear and tensile strengths. Heating the coating to 230°C caused no degradation of these properties on return to room temperature. No exudation of halocarbon was evident. Coating formulations containing 1:1, 2:1 and 3:1 ratios of silicone E2907-44-1 to halocarbon were then prepared for the wire bond stress evaluation tests.

The spray coatings were formulated as 8% solutions in toluene. The packages were fixtured by taping them in rows on a board with the tape masking the leads. The coating was sprayed four times in three passes each with

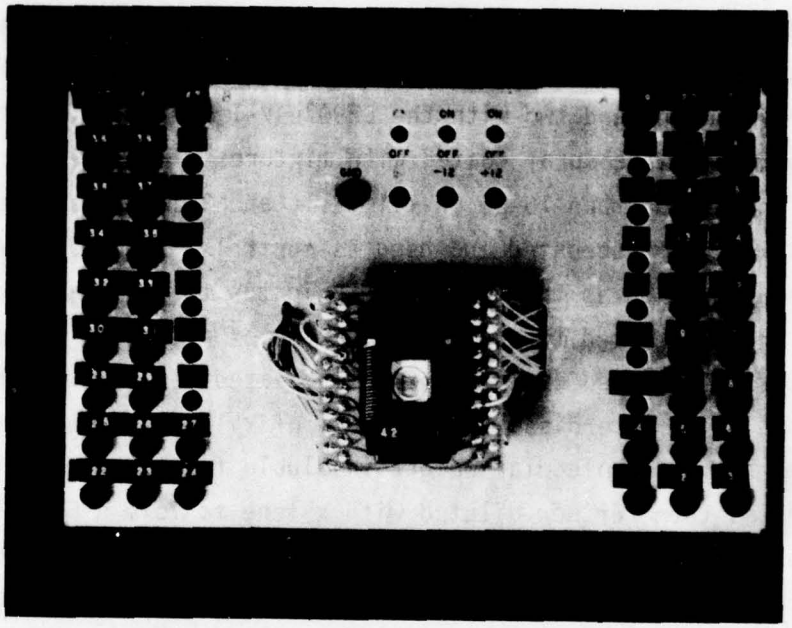


Figure 25. Test Equipment for Measurement of Bond Resistances

the board rotated 90° each time. Four coats were applied to the packages coated with DC-E2907-47-1, and to those coated with a 2 to 1 mixture of DC-E2907-44-1 and Halocarbon 15-00. Six coats were applied on the remainder of the packages. A minimum of one-half hour of air drying was used between the coatings.

Ceramic substrates taped on the boards, used for thickness measurements, were coated at the same time as the packages. The substrates and packages were air dried for one hour minimum, baked at 150°C for one hour in a nitrogen ambient, and then vacuum baked for four hours at 135°C at less than one Torr pressure.

The coating thicknesses were as follows:

a. DC-E2907-44-1: 1.5, 1.6, 1.2 mils (avg. = 1.4 mils)

b. 1 pbw 44-1 to 1 pbw halocarbon: 2.6, 1.0, 3.5 mils (avg. = 2.4 mils)

c. 2 pbw 44-1 to 1 pbw halocarbon: 1.6, 0.8, 0.9 mils (avg. = 1.1 mils)

d. 3 pbw 44-1 to 1 pbw halocarbon: 1.7, 2.1, 2.2 mils (avg. = 2.0 mils)

e. DC-E2907-47-1: Material is a gel and could not be measured with a micrometer.

The lead wires were examined visually at 30X for coating uniformity and thickness with the following results:

a. DC-E2907-47-1: As sprayed, coating thickness on 1 mil wires was about 0.5 mil. Examination of the wires after vacuum bake showed that the 47-1 coating had dewetted from the gold to form separated coating beads on the wires. No wire bridging occurred.

b. DC-E2907-44-1: Coating thickness was 0.5 to 1 mil on wires. No changes after vacuum bake and no beads of coating were noted. No wire bridging occurred.

c. 1 pbw 44-1 to 1 pbw Halocarbon: As sprayed originally, coating was 0.5 to 1 mil thick on wires, with even coating (no beading). Wires were not bridged with coating. Coating thickness reduced to nearly one-half after vacuum bake, so the packages were resprayed two more times, air dried, baked at 150°C in nitrogen, and then vacuum baked. Final lead

coating thicknesses were 0.5 to 1 mil as determined visually. Coating thickness was not noticably changed after the second vacuum bake. A few wires had beads of coating but most wires were evenly coated. The last spray applications produced bridging on some of the package wires. Bridging was distributed in the following manner:

4 packages free of bridging

1 package had 3 pairs of wires and two single wires with coating bridging from the wire to the die and to the package case

2 packages with 1 pair of bridged wires.

1 package with 1 bridged wire

d. 2 pbw 44-1 to 1 pbw Halocarbon: Coating thickness 0.5 to 1 mil before and after vacuum bake. Coating was even and coating beads were not present. None of the wires were bridged with coating.

e. 3 pbw 44-1 to 1 pbw Halocarbon: Coating thickness 0.5 to 1 mil (or possibly 1.3 mils on one side of wires), before and after vacuum bake. Wires were uniformly covered with coating, with no bead formation. One pair of bridged wires in one package, and no bridging in the other seven packages.

3.2.4.4 Results of Wire Bond Stress Evaluation

3.2.4.4.1 Electrical Tests

There were considerable differences in results between the flow coated and the spray coated packages. Flow coating resulted in bridging between some of the wires and between many of the wires and the base of the package. The packages were temperature cycled from -65°C to 150°C per MIL-STD-883A, Method 1010.1, Condition C, for 100 cycles. The electrical resistances of the bonds were measured before and after coating and after 50 and 100 temperature cycles.

The packages flow coated with DC-E2907-44-1 showed six electrical failures after 50 cycles and a cumulative total of 24 failures (~4.0%) after 100 cycles, Table 11. All failures occurred in leads bridged by the coating. The packages flow coated with DC-E2907-47-1 and the uncoated controls showed no electrical

TABLE 11. EFFECT OF TEMPERATURE CYCLING (-65 TO +150°C) ON ONE-MIL GOLD ULTRASONIC BONDS

COATING	TOTAL BONDS[1]	ELECTRICAL FAILURES[1] 50 CYCLES	ELECTRICAL FAILURES[1] 100 CYCLES	MECHANICAL[2] BOND FAILURES 100 CYCLES	MEAN BOND STRENGTH (GMS)[2] INITIAL UNCOATED	INITIAL STANDARD DEVIATION	AFTER 100 CYCLES COATED	AFTER 100 CYCLES STANDARD DEVIATION	AFTER 100 CYCLES COATING REMOVED	AFTER 100 CYCLES STANDARD DEVIATION	AFTER 100 CYCLES DEFORMED LEADS	AFTER 100 CYCLES STANDARD DEVIATION
DC-E2907-44-1 FLOW COATED	576	6	24 (14)[3]	15	5.1	0.9	5.4	0.6	5.1	1.0	4.3	1.5
DC-E2907-47-1 FLOW COATED	576	0	0	0	4.7	0.8	5.3	1.2	5.2	1.4	-	-
DC-E2907-44-1 SPRAY COATED	576	0	0	0	5.1	1.4	6.3	0.6	5.8	1.3	-	-
DC-E2907-47-1 SPRAY COATED	144[4]	0	0	0	4.8	1.2	6.0	1.5	5.9	0.9	-	-
1 PT. DC-E2907-44-1 1 PT. HALOCARBON 15-00 SPRAY COATED	576	0	7 (5)[3]	6	5.1	1.4	6.1	0.8	6.1	0.7	-	-
2 PTS. DC-E2907-44-1 1 PT. HALOCARBON 15-00 SPRAY COATED	576	0	0	0	5.0	1.3	6.1	0.5	6.0	0.7	-	-
3 PTS. DC-E2907-44-1 1 PT. HALOCARBON 15-00 SPRAY COATED	576	0	0	0	4.6	0.9	6.7	0.7	6.0	0.8	-	-
CONTROLS	576	0	0	0	4.6	0.9	5.2[5]	0.5	5.6[5]	0.8	-	-

[1]Total of 36 wires from thin-film aluminum metallized silicon chip to 42-lead ceramic package (8 packages per coating for electrical tests, 4 packages per coating for mechanical bond tests).

[2]Total of 4 packages per coating, except two for spray coated DC-E2907-47-1.

[3]Total electrical failures in 4 packages used for destructive bond tests.

[4]Total of 2 packages per coating.

[5]Not coated but subjected to the same processing parameters as the coated packages.

failures. These results indicate that bridging or encapsulation of the wires with the 44-1 coating must be avoided. Temperature cycling tests with DC-E2907-44-1 were repeated using spray applied coatings where bridging and the resultant bond failures were eliminated (Table 11). Bridging can probably be eliminated in the flow coating process by using a more dilute coating solution (less than 6.4 wt %). However, further investigation of the flow coating process was not conducted under this contract.

A photograph of one of the control circuits (after temperature cycling) is shown in Figure 26. Portions of several wires appear to be missing but are really not. This was due to lighting peculiarities. Since all packages had six leads destructively pull tested after assembly, there were 36 good wires (72 good wire bonds) in each of the control circuits both before and after the 100 temperature cycles. Pictures of typical circuits (after temperature cycling) flow coated with DC-E2907-44-1 and -47-1 are shown in Figures 27 and 28, respectively. Lead distortions resulting from 44-1 coating bridging between the wires are evident; the particular package (Figure 27) had five electrical opens after 100 temperature cycles. The packages coated with 47-1 did not show lead distortions (even with the coating bridging between the wires) or any electrical failures after temperature cycling. The 47-1 coated package (Figure 28) has light reflecting off of a coating bubble which could be mistaken for deformed leads.

The results for spray coated silicones were superior to those for flow coating. Electrical resistance measurements for pairs of wires bonded to the aluminized silicon die and to the package leads were recorded initially and after 50 and 100 temperature cycles. There were no opens and/or wires with increased resistance at 50 temperature cycles (Table 11). After 100 temperature cycles, there were seven opens in packages coated with 1 pbw 44-1 to 1 pbw halocarbon. In one package the failures all occurred on bridged wires (two center wire failures and one bond edge device failure), in another package two failures occurred on a pair of bridged wires (one center wire failure and one bond edge package failure), and in a third package there were two bond edge package failures where both of the wires were bridged but not to each other. The center wire failures were unexpected and indicate the large amount of stress which the bridged coating can apply to the wire.

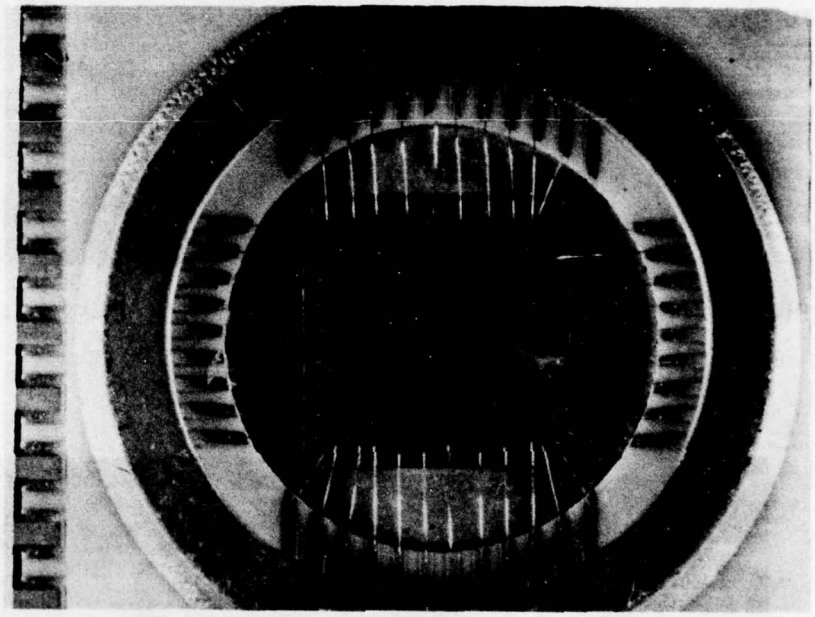


Figure 26. Bond Stress Evaluation, Control Test Circuit After 100 Temperature Cycles

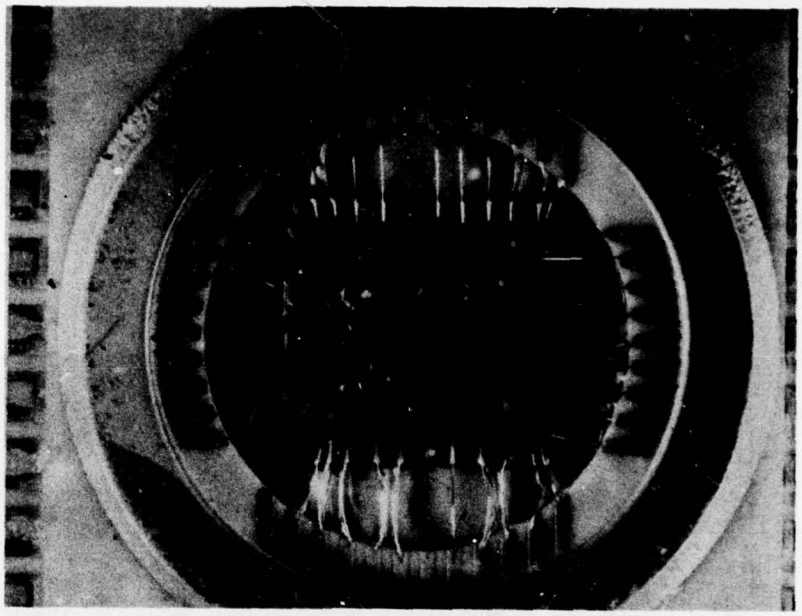


Figure 27. Bond Test Circuit Flow Coated with DC-E2907-44-1 After 100 Temperature Cycles

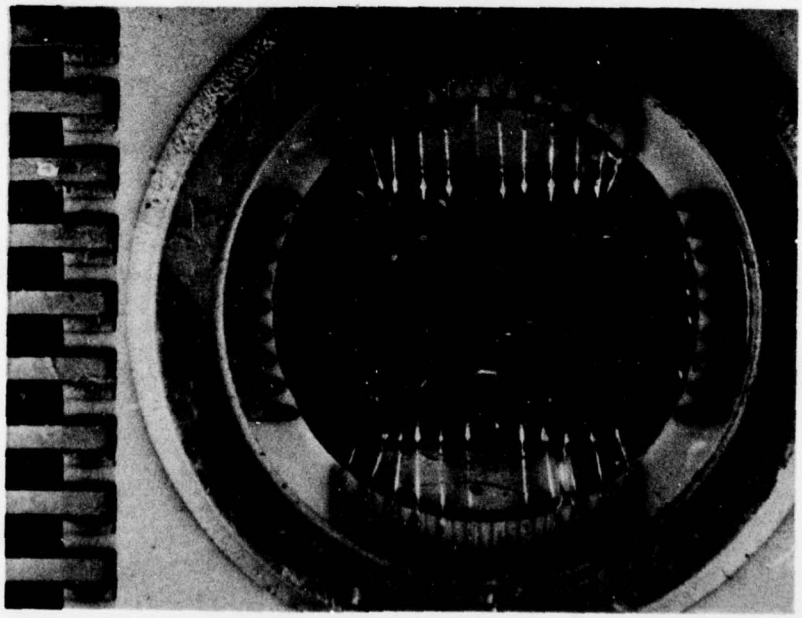


Figure 28. Bond Test Circuit Flow Coated With DC-E2907-47-1 After 100 Temperature Cycles

None of the remaining packages with the other coatings showed electrical failures after temperature cycling.

Photographs of one package with each spray coating were taken after the temperature cycling test. Figure 29 shows a test package coated with DC-E2907-47-1 while Figure 30 shows the beading of the coating on the leads due to poor wetting. Packages coated with DC-E2907-44-1, Figures 31 and 32, show good wetting of the leads and no bridging. The 2:1 mixture of the 44-1 and halocarbon coatings, Figures 33 and 34, show similar results. While one pair of wires was bridged in one of the eight packages spray coated with the 3:1 mixture (Figure 35, leads 26 and 27), no bond failures occurred and good lead wetting was observed, Figure 36. An example of the lead bridging which occurred in the packages coated with the 1:1 mixture is shown in Figure 37. Leads 5, 6, 26, 27, 37 and 38 were bridged together while leads 29 and 36 show bridging to the die and package. (Lead 5 failed after 100 cycles.) This coating also showed good lead wetting (Figure 38) with the exception of a few leads which showed some beading.

3.2.4.4.2 Humidity Tests

After completion of the temperature cycling test, half of each group of coated bond test circuits and controls were subjected to the 10-day cyclic humidity test per MIL-STD-883B, Method 1004.2, Figure 1004-1. No bias was applied to the circuits. The electrical resistances of the bonds were again measured at the conclusion of the test and the circuits were visually examined for changes in the coating or evidence of corrosion. No changes in electrical resistance occurred in any of the circuits including the controls. There were no changes in the appearance of the coatings and no evidence of corrosion when examined at 30X magnification.

3.2.4.4.3 Mechanical Tests

The remaining half of the coated bond test circuits and controls which were not subjected to humidity testing were processed as follows to evaluate the effects of the coating on the strengths of the wire bonds:

a. Six wires were destructively pull tested in each package with the coating intact. No bridged wires were pulled since they were all distorted.

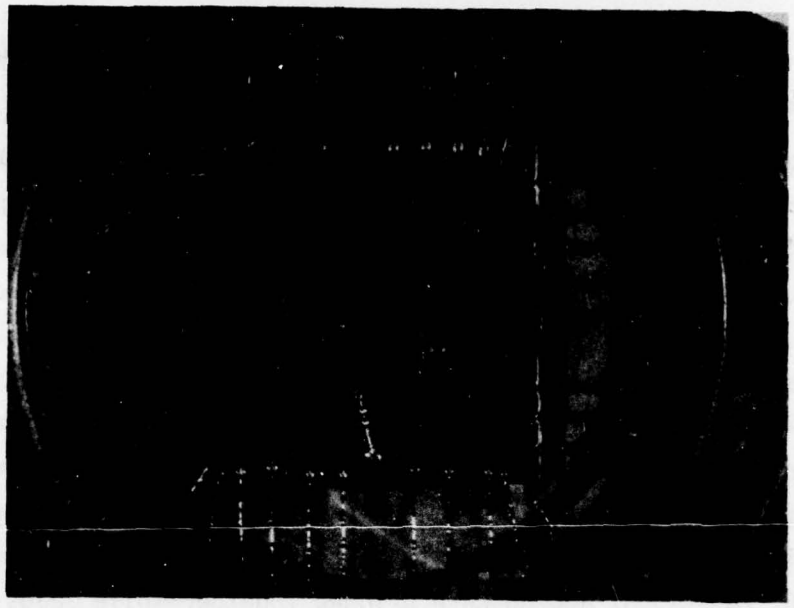


Figure 29. Bond Test Circuit No. 38, Spray Coated With DC-E2907-47-1 (10X)

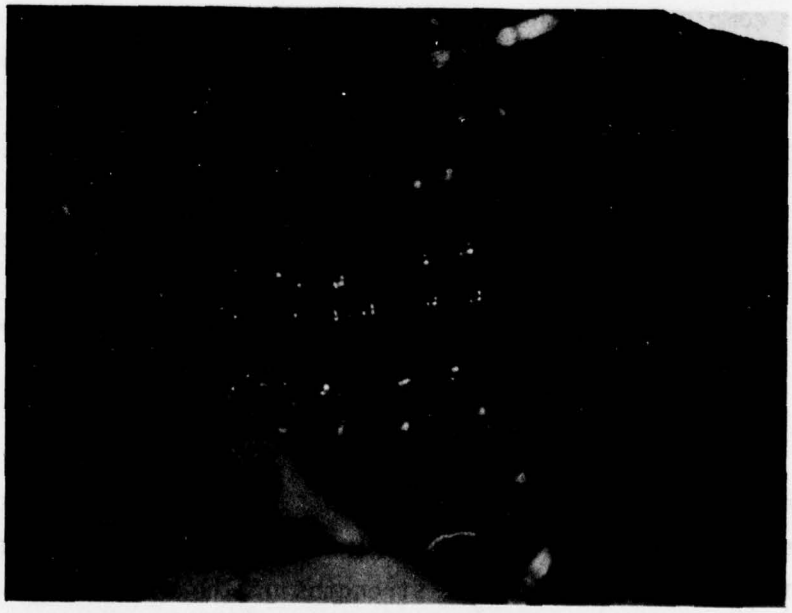


Figure 30. Wires 31 and 32 From Package No. 38 in Figure 1 (40X)

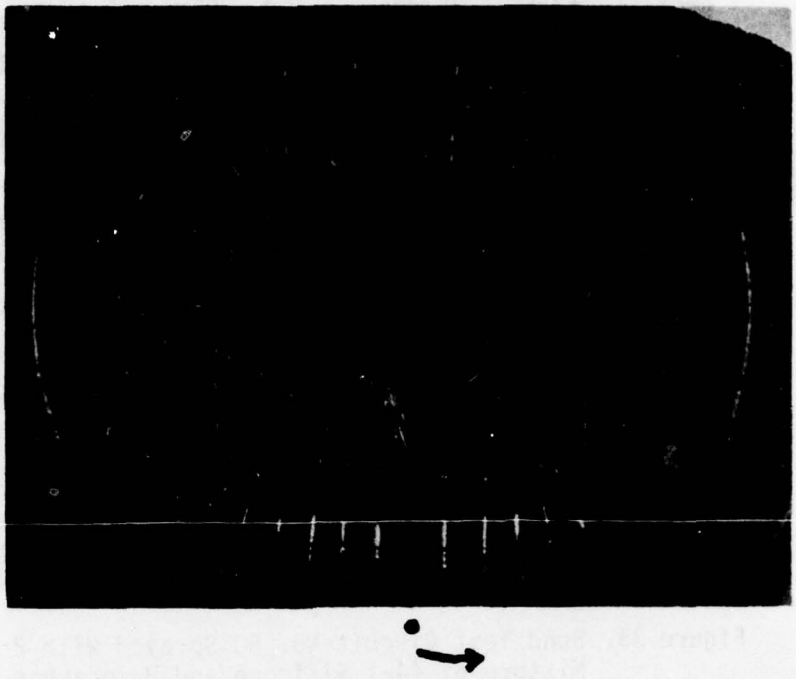


Figure 31. Bond Test Circuit No. 16 Spray Coated With DC-E2907-44-1 (10X)

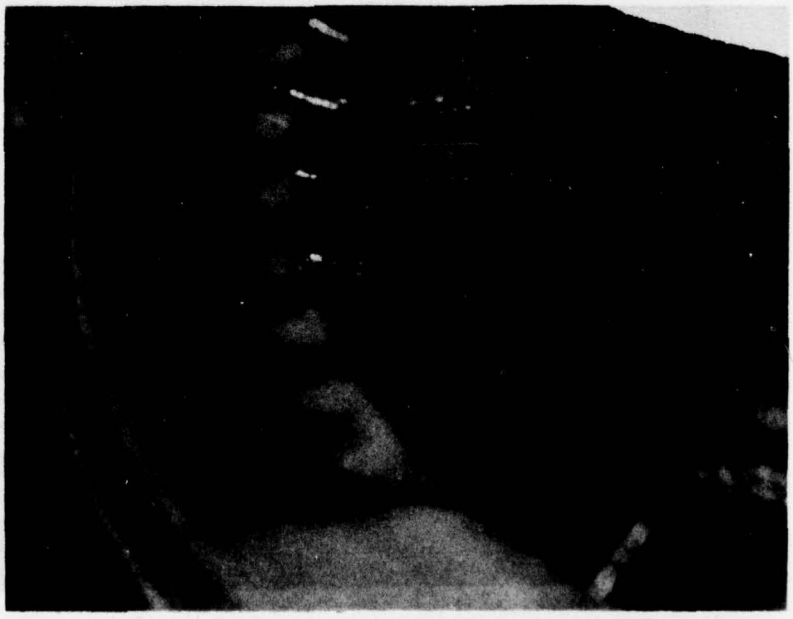


Figure 32. Wires 31 and 32 From Package No. 16 in Figure 3 (40X)

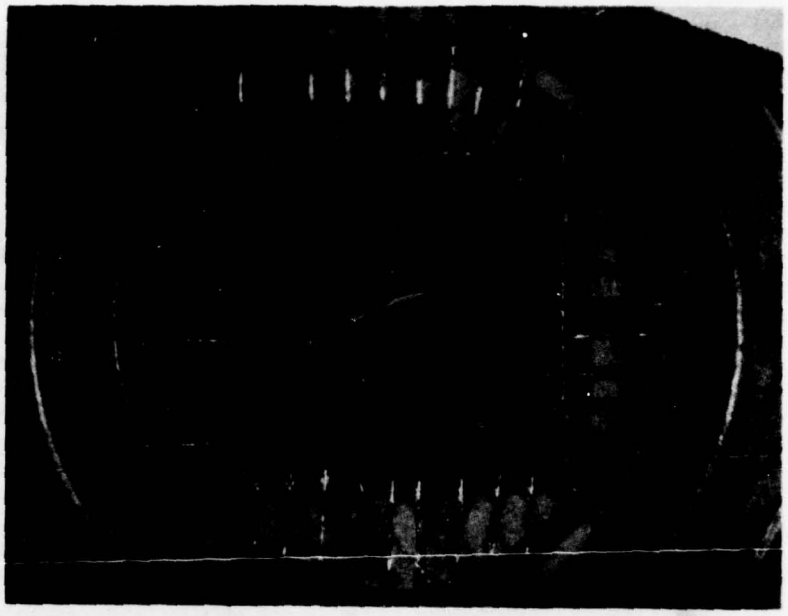


Figure 33. Bond Test Circuit No. 60 Sprayed With 2:1 Mixture of 44-1 Silicone and Halocarbon

Figure 34. Wires 41, 42, and 1 From Package No. 60 in Figure 7 (40X) - Wire No. 1 Pull Tested

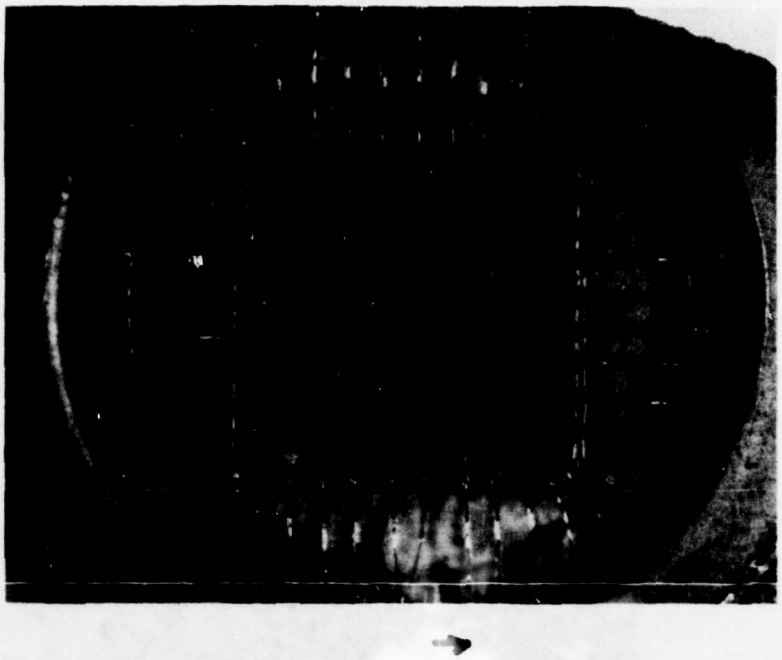


Figure 35. Bond Test Circuit No. 51 Sprayed With 3:1 Mixture of 44-1 Silicone and Halocarbon

Figure 36. Wires 30, 31, and 32 From Package No. 51 in Figure 7 (40X)

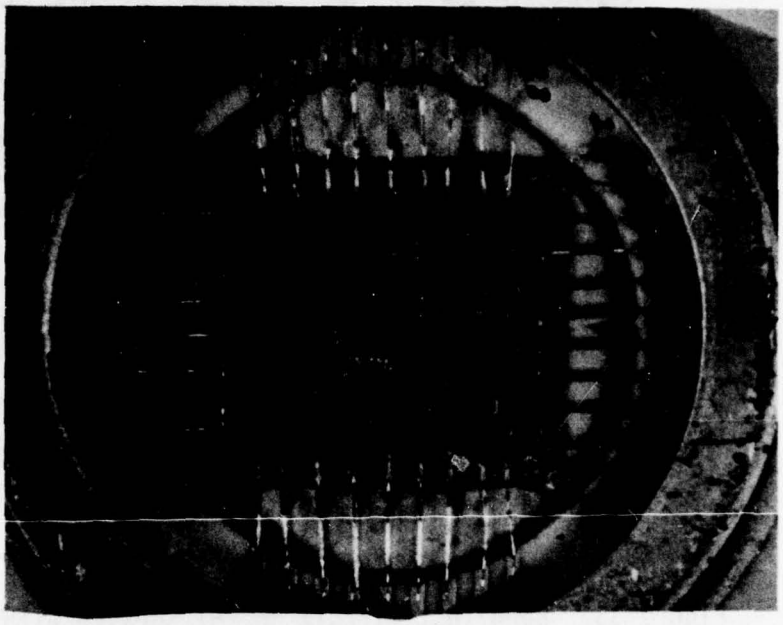


Figure 37. Bond Test Circuit No. 37 Sprayed With 1:1 Mixture of 44-1 Silicone and Halocarbon (Note distorted wires from bridging)

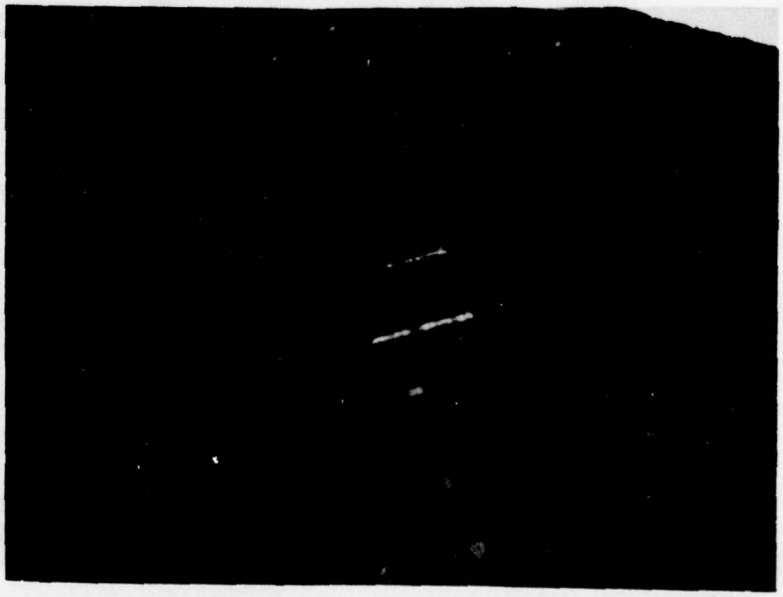


Figure 38. Wires 41, 42, and 1 From Package No. 37 in Figure 11 (40X) - Wire No. 1 Pull Tested

b. The coatings were stripped from the packages with Freon TF in a Soxhlet extractor. Twelve extraction cycles in two hours were used for all packages. The packages were examined at 30X magnification and found to be free of coating.

c. The packages were electrically tested to see if there were any changes as a result of the stripping operations. No changes in the resistances occurred except for one wire which showed increased resistance after 100 cycles. Resistance of this wire (including wire bonds and die metallization, increased from 0.2 ohms to 0.8 ohms after 100 cycles. Both resistances were in the normal range of resistance for all of the wires tested. This wire was open after the 1:1 coating had been stripped. The coating had held the wire in contact with the bonding pad and after removal of the coating, the wire was free to cause an open circuit.

d. Six wires were destructively tested in each package with the coating removed. Again, wires deformed by bridged coating were not tested.

The results are shown in Table 11. The strengths of the spray coated wires were greater in all cases than those found initially before coating. The bond strengths also remained higher than the initial values after removal of the coatings. The controls which were not coated but were subjected to the same temperature profiles and Freon TF exposure as the coated packages showed similar increases but to a lesser degree.

The failure modes of the destructively tested bonds are shown in Table 12. The increased number of center wire (CW) failures for the coated wires and for the wires after coating removal indicate a true improvement in the bond strengths.

3.2.5 Conclusions Based on Phases I and II

Based upon the tests performed in Phases I and II, the following conclusions were drawn:

a. The coatings do not degrade the wire bonds provided that bridging between the wires or from the wires to the package is eliminated. Circuits showing bridging should be stripped and recoated.

TABLE 12. DESTRUCTIVE BOND TEST FAILURE MODES OF BOND TEST SPECIMENS

Coating	Initial (Uncoated)	After 100 Cycles Coated	After 100 Cycles Coating Removal	Deformed Leads
DC-E2907-44-1 Flow Coated	6 CW[a] 17 BEP[b] 1 BED[c]	20 CW 2 BEP 2 BED	19 CW 5 BEP 1 BED	6 CW 17 BEP 1 BED
DC-E2907-47-1 Flow Coated	7 CW 15 BEP 2 BED	10 CW 7 BEP 7 BED	13 CW 7 BED 4 BEP	-
DC-E2907-44-1 Spray Coated	1 CW 14 BEP 9 BED	23 CW 1 BEP	12 CW 11 BEP 1 BED	-
DC-E2907-47-1	2 CW 10 BEP	5 CW 6 BEP 1 BED	6 CW 5 BEP 1 BED	-
1 PT. DC-E2907-44-1 1 PT. HALOCARBON 15-00 Spray Coated	6 CW 17 BEP 1 BED	23 CW 1 BEP	10 CW 10 BED 4 BEP	-
2 PTS. DC-E2907-44-1 1 PT. HALOCARBON 15-00 Spray Coated	19 BEP 3 BED 2 CBS	24 CW	19 CW 3 BED 2 BEP	
3 PTS. DC-E2907-44-1 1 PT. HALOCARBON 15-00 Spray Coated	3 CW 19 BED 2 CBS	22 CW 2 BEP	14 CW 8 BED 2 BEP	-
CONTROLS	5 CW 17 BEP 2 CBP[d]	20 CW 2 BED 2 BEP	18 CW 4 BEP 2 BED	-

[a] Center wire failure

[b] Bond edge to package failure

[c] Bond edge to device failure

[d] Complete bond to package failure

b. Spray coating is an improved method over flow coating in eliminating or minimizing bridging of wires.

c. Silicone Coating DC-E2907-43-1: This coating was dropped in the preliminary evaluations because of high outgassing. It also exhibits poor adhesion to aluminum, low cohesive strength and becomes brittle on aging.

d. Silicone Coating DC-E2907-44-1: This coating shows acceptable outgassing and electrical properties and has good tensile and adhesive strengths comparable to a crosslinked silicone. It shows good wetting of 1-mil gold wires. No bond failures occurred after 100 temperature cycles from 150°C to -65°C when spray applied. It was selected as one of the coatings to be used for coating of the hybrid test circuits.

e. Silicone Coating E2907-47-1: This coating shows the lowest outgassing but the poorest electrical properties. It shows poor wetting of 1-mil gold wires and is a tacky gel-like coating. It caused no wire bond failures even when bridging of bond wires occurred. Overall, this coating does not appear to be a good candidate.

f. Halocarbon 12-00: This low molecular weight Kel F-type material was evaluated as an additive for the silicone coatings to improve the moisture resistance. Its low melting point (approximately 120°C) and comparatively high outgassing make it a poor candidate by itself.

g. Halocarbon 15-00: This higher molecular weight Kel F-type material was also evaluated as an additive for the silicone coatings. It can be mixed in ratios of 1:1 with DC-E2907-44-1 without significantly altering the physical properties of the silicone. Its melting point of approximately 140°C is sufficient for the application. It appears to be an excellent candidate for formulation with DC-E2907-44-1.

h. Formulation 1.1 (1 pbw DC-E2907-44-1 plus 1 pbw Halocarbon 15-00: This formulation shows some dewetting properties and good physical properties. It caused wire bond failures during temperature cycling, however, making it a poor candidate.

i. Formulation 2.1 (2 pbw DC-E2907-44-1 plus 1 pbw Halocarbon 15-00): This formulation shows good physical properties and better wetting properties than formulation 1.1. It caused no bond failures on temperature cycling but is being dropped from further consideration at this time in favor of Formulation 3.1.

j. Formulation 3.1 (3 pbw DC-E2907-44-1 plus 1 pbw Halocarbon 15-00): This formulation shows good physical properties, good wetting properties and caused no bond failures. It was selected as the second coating to be used for coating of the hybrid test circuits.

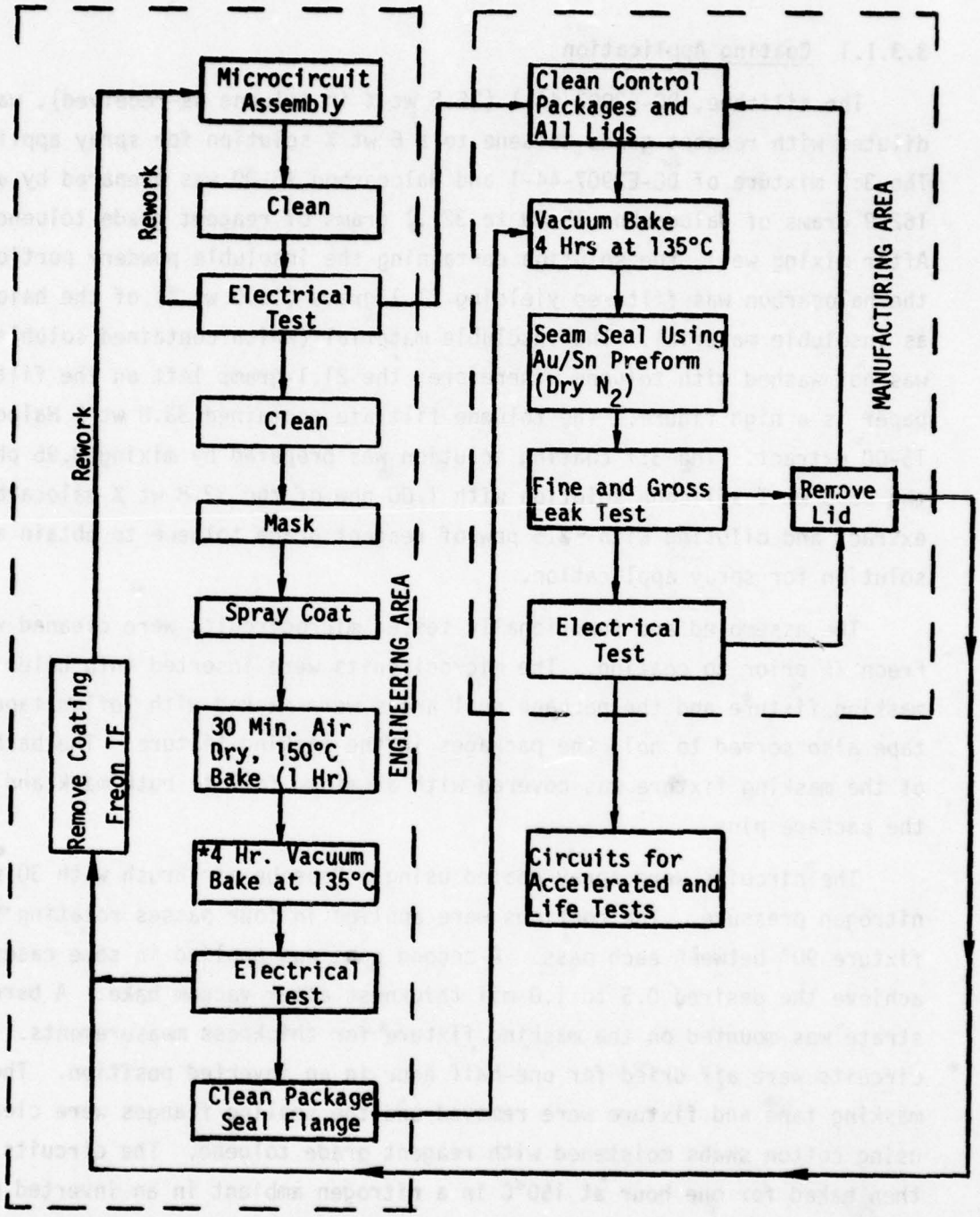
3.3 QUALIFICATION OF COATINGS (PHASE III)

3.3.1 Hybrid Microcircuit Test Vehicle Assembly

The hybrid microcircuit test vehicle selected for qualification testing of the two coatings (DC-E2907-44-1 and 3 pbw DC-E2907-44-1 plus 1 pbw halocarbon) was described in paragraph 2.3.1. The process flow for assembly, testing, coating, reworking and sealing of the microcircuits is shown in Figure 39. Assembly, coating and reworking of the microcircuits was performed by engineering personnel while testing and sealing of the circuits was performed by quality assurance and manufacturing personnel.

The devices requiring ohmic contact to the substrate were adhesive bonded with silver-filled Ablebond 36-2. The remaining devices and the substrates were adhesive bonded with Eccobond 104, a nonconductive adhesive. The devices were wire bonded to the substrates using ultrasonic bonded 1.0 mil aluminum wire. The substrates were thermal compression wire bonded to the package posts using 1.5 mil gold wire.

A total of 64 microcircuits were assembled. Sixteen of the microcircuits were prepared for delivery to the Air Force Materials Laboratory, WPAFB and the remaining 48 were divided into two equal groups for testing as shown in Figure 3.



*Precautionary extra step to avoid possible contamination of production equipment.

Figure 39. Process Flow for Assembly, Testing, Coating, Reworking and Sealing Microcircuits

3.3.1.1 Coating Application

The silicone, DC-E2907-44-1 (25.5 wt % in toluene as-received), was diluted with reagent grade toluene to a 6 wt % solution for spray application. The 3:1 mixture of DC-E2907-44-1 and Halocarbon 15-00 was prepared by adding 162.9 grams of Halocarbon 15-00 to 321.1 grams of reagent grade toluene. After mixing well, the solution containing the insoluble powdery portion of the halocarbon was filtered yielding 21.1 grams (13.0 wt %) of the halocarbon as insoluble material. The insoluble material (which contained soluble wax) was not washed with toluene, therefore, the 21.1 grams left on the filter paper is a high figure. The toluene filtrate contained 33.8 wt % Halocarbon 15-00 extract. The 3:1 coating solution was prepared by mixing 3.96 pbw of the 25.5 wt % silicone solution with 1.00 pbw of the 33.8 wt % halocarbon extract and diluting with 17.5 pbw of reagent grade toluene to obtain a 6 wt % solution for spray application.

The assembled and functionally tested microcircuits were cleaned with Freon TF prior to coating. The microcircuits were inserted into holes in a masking fixture and the package seal areas were masked with Teflon tape. The tape also served to hold the packages in the masking fixture. The backside of the masking fixture was covered with aluminum foil to both mask and ground the package pins.

The circuits were spray coated using a Paasche air brush with 30 psig nitrogen pressure. The coatings were applied in four passes rotating the fixture 90° between each pass. A second coat was applied in some cases to achieve the desired 0.5 to 1.0 mil thickness after vacuum bake. A bare substrate was mounted on the masking fixture for thickness measurements. The circuits were air dried for one-half hour in an inverted position. The masking tape and fixture were removed and the sealing flanges were cleaned using cotton swabs moistened with reagent grade toluene. The circuits were then baked for one hour at 150°C in a nitrogen ambient in an inverted position followed by vacuum baking for 4 hours at 135°C at less than one Torr pressure. (This initial vacuum bake was performed in the engineering area and was used to minimize the probability of silicone contamination of the package sealing equipment to be used in the production area.)

3.3.1.2 Rework of Coated Circuits

The coated circuits and uncoated control circuits were visually and functionally inspected prior to seal. The coating was removed from failed circuits by subjecting them to a minimum of eight extraction cycles (1.3 hours) in a Soxhlet extractor using Freon TF solvent. The circuits were then reworked and recoated in the normal manner. Seven coated circuits required rework. Three were coated with DC-E2907-44-1 and four were coated with the 3:1 silicone-halocarbon formulation. Replaced parts were primarily mesa transistors and glassivated thin film resistors. No difficulties were encountered in solvent removal of the coatings, rebonding of the devices and wires, or in recoating.

3.3.1.3 Addition of Particles to Coated Circuits

As shown in Figure 3, particles were added to one-half of the coated circuits to evaluate the ability of the coatings to protect against particle induced shorts. A total of 25 particles distributed as shown in Table 13 were added to eight circuits coated with silicone and eight coated with the 3:1 (silicone/halocarbon) mixture. A photograph of an uncoated hybrid test circuit is shown in Figure 40 and an area of a coated circuit containing the added particles is shown in Figure 41.

TABLE 13. PARTICLES ADDED TO HYBRID TEST CIRCUITS

No. of Particles	Description
5	Sn 63 solder balls, 4 to 8 mils diameter
5	Gold balls, 2 to 5 mils diameter (balls were prepared by melting the tips of gold wires and all have small pigtails)
5	Gold wire, 1 mil diameter, 4 to 8 mils long
5	Gold wire, 1 mil diameter, 8 to 16 mils long
5	Gold flakes, 4 to 10 mils (in longest dimension)

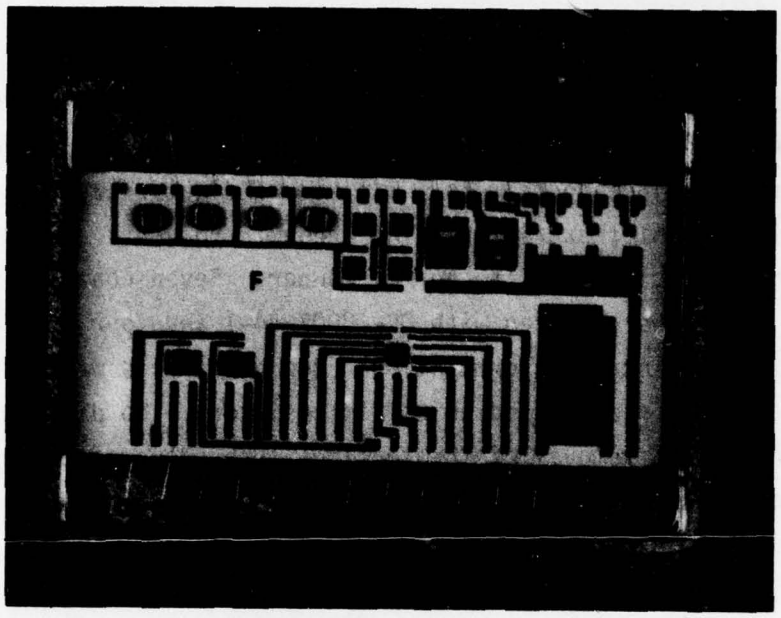


Figure 40. Photograph of Uncoated Hybrid Test Circuit

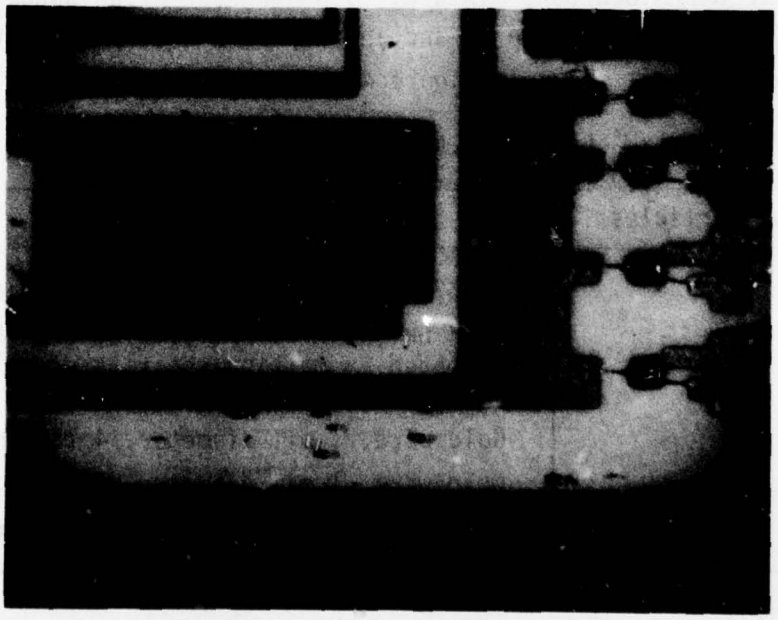


Figure 41. Photograph of Test Circuit Showing Added Particles

3.3.1.4 Package Sealing

The seal areas of the coated circuits were cleaned using a cotton swab moistened with a 50-50 mixture of reagent grade toluene and reagent grade isopropyl alcohol. The circuits were vacuum baked for 4 hours at 135°C at <1 Torr pressure, repressurized to one atmosphere with dry nitrogen and sealed using a gold-tin preform on SSEC seam sealer equipment. The sealing yield based on MIL-STD-883A, Method 1014.1, Condition A_2 (30 psig, 3 hours), and C_2 was 100% indicating no problems with coating contamination of the seal area.

3.3.2 High Stress Accelerated Test Results

A set of hybrid test specimens, distributed as shown in Figure 3, were subjected to the high stress accelerated tests shown in Figure 4. The mechanical shock and constant acceleration tests were imposed in the Y_2 direction in order to drive the particles (which were added to one-half of the coated hybrids) into the coating. This was done to determine if the particles would penetrate the coating and cause shorting of the circuitry.

All of the coated and uncoated hybrids passed the MIL-STD-883A, Method 1014.1, Condition A_2 and C_2 hermeticity tests following mechanical shock, constant acceleration, and the high temperature storage tests. All of the coated hybrids also passed the particle impact noise detection (PIND) test. One uncoated control hybrid, P/N 40527-516-46, failed the PIND test. All of the coated and control hybrids had passed the PIND test performed after sealing the packages. The coating therefore has the ability to immobilize the particles which were introduced into the packages.

The results of the electrical tests performed after the mechanical shock, constant acceleration, and high temperature storage tests are given in Tables 14 through 23. The measured electrical parameters and specification requirements are shown in Table 24. There was no evidence of particle induced shorts in any of the hybrids.

The changes in electrical parameters were within the specification limits for all of the devices with the exception of the Pd/Ag/Pd oxide thick film resistors (Tables 14 and 15). These devices are very sensitive to reducing agents such as hydrogen which has been identified as a constituent in most package ambients. The changes in resistor values appear to be both device

TABLE 14. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR UNPASSIVATED Pd/Ag/Pd OXIDE THICK FILM RESISTOR CHIPS

Coating/ Circuit No.	Resistance (ohms)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	R_1	R_2	R_1	R_2	R_1	R_2	R_1	R_2
DC-E2907-44-1 (NP[e])								
40527-516-8	427.5	480.0	427.5	480.0	194.5	338.2	191.0	322.0
-9	440.5	466.0	440.5	466.0	450.0	306.0	452.0	301.5
-16	451.0	462.5	451.0	462.5	233.5	210.5	216.5	194.8
-69	451.5	434.5	452.0	435.0	59.36	155.5	57.99	151.0
Avg. % Change (NP)	-		+0.02		-46.1		-3.14	
DC-E2907-44-1 (WP[f])								
40527-516-4	457.0	438.0	458.5	440.0	336.0	285.5	328.0	282.5
-12	443.0	456.5	444.5	458.5	244.0	415.5	236.8	403.6
-21	484.5	475.0	486.0	476.5	69.0	254.5	68.5	246.0
-30	454.3	429.5	456.0	431.0	150.5	202.5	142.6	197.5
Avg % Change (WP)	-		+0.37		-46.2		-2.66	
Avg % Change Overall	-		+0.20		-46.2		-2.90	
3 to 1 Mixture (NP)								
40527-516-14	441.5	432.5	441.5	432.5	455.0	435.5	461.5	440.5
-18	431.0	480.5	432.5	482.0	434.5	486.1	442.4	494.0
-23	466.5	447.5	466.5	447.5	312.0	195.5	303.5	190.0
-33	475.0	456.2	475.0	456.0	371.0	361.9	360.9	354.0
Avg % Change (NP)	-		+0.09		-16.0		-0.14	
3 to 1 Mixture (WP)								
40527-516-11	440.5	438.0	442.0	439.6	260.5	289.0	256.6	286.2
-19	433.5	439.3	435.0	441.0	346.4	313.0	338.6	308.4
-38	457.0	450.5	458.5	452.0	233.5	299.0	226.5	287.0
-50	452.5	424.0	454.0	425.8	46.95	71.1	48.52	73.00
Avg % Change (WP)	-		+0.36		-47.4		-1.86	
Avg % Change Overall	-		+0.22		-31.7		-1.00	
Uncoated Controls (NP)								
40527-516-17	454.5	459.0	455.0	475.0	174.0	106.0	180.0	110.5
-24	458.5	465.0	458.5	464.8	274.3	324.5	276.9	326.5
-27	460.0	472.0	460.0	472.0	280.5	248.5	287.5	254.5
-28	459.0	426.0	458.5	426.0	419.5	260.5	425.5	265.5
-37	446.0	478.5	447.3	479.0	121.0	273.4	123.0	275.0
-46	448.5	437.1	448.5	437.0	450.1	438.5	458.5	446.5
-60	428.0	448.5	428.0	448.5	430.0	450.5	438.5	458.5
-78	427.0	444.5	427.0	441.9	336.0	214.5	342.0	218.3
Avg. % Change	-		+0.20		-33.4		+1.78	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

TABLE 15. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR PASSIVATED Pd/Ag/Pd OXIDE THICK FILM RESISTOR CHIPS

Coating/ Circuit No.	Resistance (ohms)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	R_3	R_4	R_3	R_4	R_3	R_4	R_3	R_4
DC-E2907-44-1 (NP[e])								
40527-516-8	454.8	412.0	455.0	412.0	443.0	411.0	445.0	420.5
-9	384.0	429.1	384.0	429.0	344.3	417.5	341.5	405.0
-16	408.0	396.5	407.8	396.1	342.0	395.5	348.0	422.5
-69	436.7	420.7	436.5	420.5	424.4	394.5	431.5	399.5
Avg. % Change (NP)	-		-0.02		-5.08		+1.31	
DC-E2907-44-1 (WP[f])								
40527-516-4	421.0	384.5	422.5	386.0	425.0	386.0	427.5	394.0
-12	416.5	418.1	418.0	420.0	418.0	419.5	425.0	428.5
-21	421.3	437.5	423.0	439.0	344.5	435.0	348.5	443.0
-30	412.5	423.5	414.0	425.0	332.3	314.0	325.0	309.6
Avg % Change (WP)	-		+0.36		-7.82		+0.87	
Avg % Change Overall	-		+0.17		-6.45		+1.09	
3 to 1 Mixture (NP)								
40527-516-14	398.5	395.0	399.0	395.5	392.0	323.5	400.0	329.0
-18	423.1	397.9	425.0	399.5	427.5	398.4	436.5	408.0
-23	423.0	424.0	423.0	424.0	392.0	299.0	400.0	299.5
-33	424.0	406.5	424.0	406.7	288.4	316.5	291.5	315.5
Avg % Change (NP)	-		+0.15		-13.8		+1.49	
3 to 1 Mixture (WP)								
40527-516-11	441.0	459.0	442.5	460.5	389.0	443.0	394.0	449.0
-19	423.6	397.5	425.5	399.3	425.5	400.4	434.0	408.0
-38	429.0	406.0	431.0	408.5	412.5	348.8	415.5	353.5
-50	420.5	430.0	422.0	431.5	317.0	427.5	315.1	434.9
Avg % Change (WP)	-		+0.42		-7.14		+1.29	
Avg % Change Overall	-		+0.29		-10.5		+1.39	
Uncoated Controls (NP)								
40527-516-17	461.5	414.0	461.5	1.332[g]	360.0	1.364[g]	368.5	1.361[g]
-24	395.0	411.8	395.0	411.5	247.5	346.0	254.1	353.5
-27	425.0	422.5	425.5	422.9	310.1	268.3	318.0	274.5
-28	427.5	462.5	428.0	462.2	261.8	435.5	268.5	444.5
-37	401.0	391.4	402.0	391.5	222.0	287.0	226.9	293.0
-46	415.5	449.0	415.5	449.0	414.5	449.5	424.0	458.5
-60	446.5	406.5	446.0	406.5	446.5	406.5	455.0	416.0
-78	393.5	418.0	393.5	418.0	369.3	274.0	377.5	280.0
Avg. % Change	-		+0.14		-19.6		+2.24	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

[g] Failed device, not included in average % change at time failure occurred

TABLE 16. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR PASSIVATED NiCr THIN FILM RESISTOR CHIPS

Coating/ Circuit No.	Resistance (K ohms)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	R_5	R_6	R_5	R_6	R_5	R_6	R_5	R_6
DC-E2907-44-1 (NP[e])								
40527-516-8	496.9	497.0	496.5	496.6	499.0	498.9	507.4	507.0
-9	-	498.5	-	498.5	-	500.5	-	508.5
-16	496.5	496.5	496.5	496.5	498.9	499.0	506.5	506.5
-69	496.3	496.5	496.5	496.5	498.5	498.5	506.5	506.3
Avg. % Change (NP)	-		-0.02		+0.43		+1.59	
DC-E2907-44-1 (WP[f])								
40527-516-4	491.1	491.0	496.2	496.0	499.0	499.0	506.5	506.0
-12	491.2	491.0	496.5	496.5	499.4	499.1	507.0	506.5
-21	491.0	491.0	496.1	496.0	499.0	499.0	506.5	506.5
-30	491.4	490.5	496.4	496.0	499.4	498.5	507.0	506.5
Avg % Change (WP)	-		+1.06		+1.64		+1.51	
Avg % Change Overall	-		+0.52		+0.74		+1.55	
3 to 1 Mixture (NP)								
40527-516-14	497.4	497.4	496.5	496.5	498.9	499.0	506.0	506.0
-18	494.5	494.5	496.5	496.8	499.0	499.5	506.4	506.3
-23	497.2	497.1	496.5	496.5	498.5	498.5	506.0	506.0
-33	497.0	497.5	496.5	496.4	498.3	499.0	506.0	506.5
Avg % Change (NP)	-		-0.02		+0.44		+1.47	
3 to 1 Mixture (WP)								
40527-516-11	490.9	491.0	496.0	496.0	499.0	499.0	506.5	506.5
-19	490.9	491.0	496.0	496.5	499.3	499.5	506.9	507.0
-38	-	-	-	-	-	-	-	-
-50	491.0	493.0	496.0	498.5	498.9	501.0	506.8	509.0
Avg % Change (WP)	-		+1.06		+1.67		+1.52	
Avg % Change Overall	-		+0.52		+1.06		+1.50	
Uncoated Controls (NP)								
40527-516-17	496.4	497.0	496.4	497.2	498.6	499.5	506.4	507.0
-24	496.5	496.5	496.2	496.5	497.9	498.2	505.5	505.6
-27	496.7	529.3	496.5	528.0	498.9	529.5	506.2	539.5
-28	497.0	496.5	496.5	496.5	499.0	498.5	506.5	506.0
-37	490.5	490.0	496.4	496.5	498.6	498.5	506.9	506.5
-46	497.0	496.5	497.3	496.5	499.5	498.5	506.5	505.4
-60	499.6	499.0	492.5	491.5	499.5	499.0	506.8	506.0
-78	498.6	499.0	488.5	499.0	500.5	500.5	508.5	508.0
Avg. % Change	-		-0.18		+0.48		+1.15	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

TABLE 17. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR UNPASSIVATED NiCr THIN FILM RESISTOR CHIPS

Coating/ Circuit No.	Resistance (K ohms)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	R_7	R_8	R_7	R_8	R_7	R_8	R_7	R_8
DC-E2907-44-1 (NP[e])								
40527-516-8	487.0	495.8	487.4	495.8	490.0	498.5	498.0	507.0
-9	510.7	482.5	511.0	482.0	513.4	484.6	522.0	492.5
-16	342.8	482.0	344.0	482.0	346.3	484.5	353.3	492.0
-69	488.5	491.5	489.4	492.0	491.5	494.0	499.5	502.0
Avg. % Change (NP)	-		+0.09		+0.59		+1.66	
DC-E2907-44-1 (WP[f])								
40527-516-4	474.3	498.0	479.5	502.7	482.6	506.0	489.5	513.0
-12	468.3	491.5	473.5	496.0	476.7	499.5	484.0	507.0
-21	475.5	478.0	481.0	482.0	484.0	485.0	491.5	492.5
-30	498.5	484.5	504.5	489.0	507.7	492.0	515.8	500.0
Avg % Change (WP)	-		+1.01		+1.67		+1.54	
Avg % Change Overall	-		+0.55		+1.13		+1.60	
3 to 1 Mixture (NP)								
40527-516-14	482.0	487.5	482.0	487.0	484.5	490.0	491.5	497.0
-18	506.0	497.5	508.5	499.5	512.0	503.0	519.4	510.0
-23	477.0	501.0	476.5	500.5	479.2	503.4	486.5	510.5
-33	475.0	477.3	474.9	476.5	477.5	479.0	484.5	486.1
Avg % Change (NP)	-		+0.06		+0.66		+1.44	
3 to 1 Mixture (WP)								
40527-516-11	489.5	484.5	495.1	489.0	498.5	492.0	506.1	499.5
-19	490.5	491.5	496.0	496.0	499.5	499.4	507.0	506.5
-38	471.0	476.9	476.5	481.0	479.5	484.0	486.5	491.5
-50	491.0	493.8	496.9	498.1	500.0	501.0	508.0	509.0
Avg % Change (WP)	-		+1.03		+1.67		+1.53	
Avg % Change Overall	-		+0.55		+1.16		+1.49	
Uncoated Controls (NP)								
40527-516-17	478.5	483.5	479.0	483.5	481.5	486.0	489.0	493.4
-24	480.5	482.7	480.5	482.5	482.5	484.5	489.6	491.5
-27	482.0	483.0	482.0	483.0	484.6	484.5	491.5	492.5
-28	490.0	494.0	490.0	494.0	492.5	496.5	500.0	503.5
-37	512.5	485.5	512.0	485.5	514.5	487.9	523.0	495.5
-46	508.5	342.8	508.9	342.5	511.5	344.1	518.5	349.0
-60	486.5	486.0	486.8	486.0	490.2	489.5	497.0	496.0
-78	483.0	494.5	483.0	494.1	485.0	496.0	493.0	504.0
Avg. % Change	-		0.00		+0.49		+1.50	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

TABLE 18. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR UNPASSIVATED 2N4391 JFETs, ZERO GATE VOLTAGE DRAIN CURRENT

Coating/ Circuit No.	I_{DSS} (ma)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	Q_3	Q_4	Q_3	Q_4	Q_3	Q_4	Q_3	Q_4
DC-E2907-44-1 (NP[e])								
40527-516-8	99.4	109.3	99.9	109.9	99.3	109.0	73.5	81.9
-9	67.2	76.8	67.9	77.7	68.7	78.1	50.5	57.3
-16	110.0	76.0	110.0	76.3	109.0	75.8	80.7	58.6
-69	104.9	53.2	105.4	53.7	104.3	53.6	78.2	39.2
Avg. % Change (NP)	-		+0.57		+0.15		-25.5	
DC-E2907-44-1 (WP[f])								
40527-516-4	63.5	71.9	66.5	74.9	66.2	74.6	49.8	56.1
-12	66.6	90.0	69.4	92.8	69.1	92.3	50.3	68.2
-21	88.0	96.7	90.6	99.3	89.7	97.8	66.7	73.2
-30	81.0	100.9	84.0	104.0	83.5	103.7	61.8	77.5
Avg % Change (WP)	-		+3.47		+2.77		-25.6	
Avg % Change Overall	-		+2.02		+1.46		-25.6	
3 to 1 Mixture (NP)								
40527-516-14	54.8	59.8	56.9	61.8	56.9	62.2	43.9	48.4
-18	67.9	69.1	70.7	72.1	70.0	71.3	51.7	52.9
-23	76.2	66.0	77.9	67.8	77.7	67.7	57.0	73.3
-33	83.1	79.3	85.2	81.5	84.3	80.5	61.7	59.2
Avg % Change (NP)	-		+3.18		+2.59		-31.8	
3 to 1 Mixture (WP)								
40527-516-11	80.0	89.7	82.8	92.4	82.4	91.7	60.6	67.9
-19	93.7	97.7	100.6	96.5	95.7	99.8	72.9	75.6
-38	100.5	58.7	103.3	61.6	102.5	61.3	76.8	44.6
-50	67.9	72.3	70.9	75.4	70.4	74.7	52.0	55.1
Avg % Change (WP)	-		+3.49		+2.73		-25.5	
Avg % Change Overall	-		+3.34		+2.66		-28.7	
Uncoated Controls (NP)								
40527-516-17	65.2	97.0	65.5	97.3	65.1	96.6	48.3	72.3
-24	105.9	109.8	106.5	110.7	106.4	109.9	79.8	82.7
-27	94.2	51.7	94.3	52.1	93.1	51.6	70.2	37.7
-28	74.2	93.8	74.6	94.2	74.1	93.2	54.9	70.7
-37	87.6	80.0	88.0	80.4	87.1	80.0	63.9	59.2
-46	59.5	89.6	59.8	90.0	59.5	89.7	43.6	66.4
-60	95.0	103.9	95.2	104.2	95.2	104.6	70.1	78.1
-78	97.7	52.6	97.8	53.1	96.3	52.4	71.6	37.9
Avg. % Change	-		+0.44		-0.22		-25.6	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

TABLE 19. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR PASSIVATED 2N4391 JFETs, ZERO GATE VOLTAGE DRAIN CURRENT

Coating/ Circuit No.	I_{DSS} (ma)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	Q_5	Q_6	Q_5	Q_6	Q_5	Q_6	Q_5	Q_6
DC-E2907-44-1 (NP[e])								
40527-516-8	72.3	73.4	73.1	74.2	72.7	73.7	53.5	54.2
-9	54.3	66.4	55.1	67.3	55.8	67.9	41.5	49.4
-16	63.0	60.2	63.3	60.6	63.1	60.3	47.9	43.1
-69	62.8	60.8	63.5	61.3	63.2	61.5	46.4	45.0
Avg. % Change (NP)	-		+1.01		+0.98		-26.5	
DC-E2907-44-1 (WP[f])								
40527-516-4	63.5	40.6	66.5	43.6	65.8	43.2	48.5	31.6
-12	65.2	58.5	68.2	61.6	67.3	60.9	49.1	44.2
-21	59.1	63.8	61.8	66.4	61.2	65.9	44.6	47.9
-30	59.3	63.5	62.5	66.6	62.0	65.8	45.0	47.9
Avg % Change (WP)	-		+5.00		+3.92		-27.1	
Avg % Change Overall	-		+3.01		+2.45		-26.8	
3 to 1 Mixture (NP)								
40527-516-14	78.8	81.4	80.9	83.4	80.2	82.8	62.2	64.6
-18	70.8	60.6	73.7	63.5	73.3	62.5	55.2	46.1
-23	66.9	62.3	68.6	64.1	68.8	64.2	50.3	47.1
-33	63.7	40.3	65.9	42.6	65.3	42.4	47.3	30.2
Avg % Change (NP)	-		+3.41		+2.80		-25.3	
3 to 1 Mixture (WP)								
40527-516-11	66.9	66.2	69.8	69.1	68.5	68.5	49.8	49.8
-19	53.6	59.3	56.8	62.9	56.3	62.7	43.2	46.6
-38	57.5	71.8	60.5	74.8	59.8	73.8	43.3	53.8
-50	37.9	57.2	41.0	60.3	40.7	59.9	29.3	44.4
Avg % Change (WP)	-		+5.17		+4.20		-26.5	
Avg % Change Overall	-		+4.29		+3.50		-25.9	
Uncoated Controls (NP)								
40527-516-17	61.3	41.1	61.7	41.6	60.9	41.2	44.9	30.1
-24	66.6	55.9	67.2	56.7	67.2	56.8	49.4	41.7
-27	67.6	77.7	68.1	78.2	66.2	76.7	48.5	56.3
-28	62.3	62.2	62.8	62.8	61.8	62.3	45.2	45.8
-37	47.2	61.3	47.7	61.7	47.3	61.2	34.1	44.4
-46	72.3	72.6	72.9	73.2	73.4	73.0	54.7	54.5
-60	99.0	54.9	99.4	55.3	99.0	55.8	73.2	42.0
-78	61.1	67.4	61.5	67.9	60.7	66.8	45.5	48.7
Avg. % Change	-		+0.79		-0.02		-26.3	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

TABLE 20. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR LM741 OP AMPS, OFFSET VOLTAGE

Coating/ Circuit No.	Offset Voltage (mv)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	Z_1	Z_2	Z_1	Z_2	Z_1	Z_2	Z_1	Z_2
DC-E2907-44-1 (NP[e])								
40527-516-8	4.054	0.6933	4.192	0.7922	4.335	0.8571	4.359	1.293
-9	3.058	0.4390	3.108	0.5198	3.149	0.4304	4.950	1.031
-16	0.7992	1.803	1.118	1.942	1.075	1.892	2.066	3.223
-69	1.983	0.2481	2.252	0.2429	2.175	0.2241	2.398	0.5532
Avg. % Change (NP)	-		+10.6		+8.07		+40.6	
DC-E2907-44-1 (WP[f])								
40527-516-4	2.341	2.218	2.315	2.334	2.152	2.194	3.139	3.137
-12	1.849	3.173	1.608	3.103	1.562	3.063	2.286	5.178
-21	1.149	2.618	1.313	2.835	1.195	2.573	1.902	4.176
-30	1.732	2.474	1.656	2.281	1.566	2.212	2.625	3.499
Avg % Change (WP)	-		-0.59		-5.88		+57.0	
Avg % Change Overall	-		+5.01		+1.10		+48.8	
3 to 1 Mixture (NP)								
40527-516-14	5.541	0.7313	5.683	0.8381	5.594	0.5439	2.317	1.059
-18	1.323	0.7233	1.456	0.7692	1.339	0.7101	2.397	1.234
-23	1.684	1.855	1.616	1.865	1.639	1.808	2.461	2.076
-33	2.380	2.093	2.503	2.116	2.223	1.749	3.628	3.608
Avg % Change (NP)	-		-3.18		-4.41		+20.3	
3 to 1 Mixture (WP)								
40527-516-11	1.751	-0.1238	0.6130	-0.1787	1.861	-0.2489	3.026	0.1335
-19	3.083	-0.2208	2.991	-0.2353	2.997	-0.3721	4.783	-0.1663
-38	3.952	1.114	3.870	0.8591	3.813	0.8531	5.916	1.347
-50	-1.021	0.7982	-1.207	0.5054	-1.092	0.4708	-1.120	0.7013
Avg % Change (WP)	-		-13.3		-2.98		+46.9	
Avg % Change Overall	-		-8.24		-3.70		+33.6	
Uncoated Controls (NP)								
40527-516-17	0.4989	0.9950	0.5934	1.191	0.5274	0.9930	1.352	1.539
-24	0.7382	2.924	0.6776	2.792	0.6663	2.719	1.970	4.463
-27	1.372	2.326	1.521	2.477	1.446	2.307	2.596	2.880
-28	-1.352	1.697	-1.110	1.772	-1.233	1.712	-1.252	2.906
-37	-0.1846	0.8381	-0.0889	1.304	-0.1185	1.083	0.4701	2.451
-46	2.518	3.410	2.508	3.419	2.544	3.315	4.282	4.652
-60	0.5636	-0.1039	0.7455	0.0183	0.7282	-0.1143	1.343	1.062
-78	0.8871	1.695	0.9630	1.572	0.8201	1.547	1.052	2.013
Avg. % Change	-		+18.4		-1.04		+65.9	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

TABLE 21. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR MESA TRANSISTORS, COLLECTOR-EMITTER CUTOFF CURRENT

Coating/ Circuit No.	I_{CEX} (mA)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
DC-E2907-44-1 (NP[e])								
40527-516-8	0.0039	0.0005	0.0002	0.0001	0.0003	0.0001	0.0120	0.0127
-9	0.0560	0.0004	0.0293	0.0001	0.0004	0.0003	0.1823	0.0110
-16	0.0034	0.0004	0.0001	0.0001	0.0001	0.0001	0.0133	0.0163
-69	-	0.0005	-	0.0001	-	0.0001	-	0.0104
Avg. % Change (NP)	-		-53.9		-97.9		+18,429	
DC-E2907-44-1 (WP[f])								
40527-516-4	0.0011	0.8189	0.0001	0.1945	0.0004	0.7846	0.0213	0.6885
-12	0.0012	0.0020	0.0003	0.0010	0.0003	0.0001	0.0104	0.0180
-21	0.0027	0.0021	0.0011	0.0008	0.0004	0.0001	0.0235	0.0191
-30	0.0025	0.0111	0.0013	0.0069	0.0004	0.0005	0.0328	0.0958
Avg % Change (WP)	-		-75.5		-6.51		+15.6	
Avg % Change Overall	-		-64.7		-52.2		+9,223	
3 to 1 Mixture (NP)								
40527-516-14	0.0065	0.0004	0.0055	0.0003	0.2437	0.0002	0.0279	0.0084
-18	0.0002	0.0001	0.0001	0.0001	0.0005	0.0004	0.0535	0.0357
-23	0.3486	0.0057	0.3239	0.0044	0.3983	0.0006	0.2603	0.1187
-33	0.0244	0.0564	0.0415	0.0393	0.0006	0.0206	0.0171	0.4438
Avg % Change (NP)	-		-6.15		+50.3		+45.2	
3 to 1 Mixture (WP)								
40527-516-11	0.0011	0.0012	0.0001	0.0005	0.0003	0.0002	0.0127	0.0138
-19	0.0078	0.0079	0.0043	0.0053	0.0002	0.0002	0.0290	0.0422
-38	0.0011	0.0008	0.0002	0.0002	0.0001	0.0001	0.0088	0.0129
-50	0.0062	0.0010	0.0034	0.0002	0.0004	0.0001	0.0554	0.0172
Avg % Change (WP)	-		-47.6		-94.1		+12,000	
Avg % Change Overall	-		-26.9		-21.9		+6,023	
Uncoated Controls (NP)								
40527-516-17	0.1888	0.0009	0.2082	0.0004	0.2095	0.0001	0.2316	0.0138
-24	0.0114	0.0134	0.0103	0.0126	0.0001	0.0119	0.0982	0.1158
-27	0.0032	-	0.0005	-	0.0004	-	0.0125	-
-28	0.0180	0.0005	0.0174	0.0001	0.0003	0.0004	0.0149	0.0152
-37	0.0004	0.0003	0.0003	0.0003	0.0001	0.0001	0.0175	0.0209
-46	0.0032	0.0084	0.0002	0.0218	0.0008	0.1729	0.0405	0.2688
-60	-	-	-	-	-	-	-	-
-78	0.0034	0.0013	0.0007	0.0009	0.0004	0.0002	0.0324	0.0761
Avg. % Change	-		+8.10		+56.9		+241	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

TABLE 22. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR 2NC5975 MESA TRANSISTORS, DC CURRENT GAIN

Coating/ Circuit No.	h_{FE}							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
DC-E2907-44-1 (NP[e])								
40527-516-8	120.1	120.1	119.7	119.8	118.0	118.4	109.7	110.2
-9	104.9	128.7	103.4	128.3	104.9	118.0	118.4	121.9
-16	121.1	122.3	119.9	122.0	118.9	119.9	111.1	113.7
-69	128.0	129.0	127.7	128.7	125.0	127.1	121.3	122.9
Avg. % Change (NP)	-		-0.49		-2.46		-2.23	
DC-E2907-44-1 (WP[f])								
40527-516-4	124.7	124.3	124.0	123.7	118.3	120.6	115.6	117.3
-12	120.2	121.0	120.8	120.3	119.8	120.1	112.7	112.1
-21	126.2	121.6	125.7	120.9	124.5	120.5	119.6	112.1
-30	123.2	133.3	122.6	132.5	122.1	132.0	117.2	127.0
Avg % Change (WP)	-		-0.40		-1.69		-4.50	
Avg % Change Overall	-		-0.45		-2.08		-3.37	
3 to 1 Mixture (NP)								
40527-516-14	127.0	126.5	126.8	126.1	123.6	123.3	121.6	123.4
-18	119.9	120.9	119.6	123.0	122.1	125.9	118.0	124.6
-23	131.3	120.0	130.8	120.8	122.0	116.8	123.9	115.3
-33	127.1	129.9	126.8	129.4	125.3	126.7	121.4	123.3
Avg % Change (NP)	-		+0.08		-1.68		-1.43	
3 to 1 Mixture (WP)								
40527-516-11	121.9	124.2	121.3	123.6	124.2	122.2	120.2	117.4
-19	123.0	124.9	122.5	124.2	119.3	120.8	116.0	120.9
-38	122.3	129.0	120.4	128.4	117.3	122.7	114.4	122.4
-50	133.5	127.4	132.8	126.8	128.5	125.4	126.4	122.2
Avg % Change (WP)	-		-0.64		-2.54		-2.13	
Avg % Change Overall	-		-0.28		-2.11		-1.78	
Uncoated Controls (NP)								
40527-516-17	127.9	126.9	127.4	126.5	126.9	125.8	123.1	122.1
-24	130.3	119.4	129.7	118.9	136.9	121.0	129.6	120.2
-27	123.5	125.8	123.0	125.4	123.8	136.8	119.3	130.8
-28	123.0	127.0	121.2	126.6	137.5	128.7	125.0	128.3
-37	120.4	121.5	121.5	121.3	144.8	128.7	115.7	117.0
-46	128.2	125.7	127.7	125.2	127.4	124.7	123.2	122.4
-60	123.2	132.0	122.9	131.6	122.5	131.1	117.6	126.3
-78	125.6	132.1	125.2	131.7	135.4	133.9	123.8	129.5
Avg. % Change	-		-0.32		+3.63		-5.37	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

TABLE 23. MECHANICAL AND HIGH TEMPERATURE STORAGE TEST RESULTS FOR CD4001 CMOS, QUIESCENT CURRENT

Coating/ Circuit No.	I_{DD} (na)							
	Mech. Shock[a] & Constant Accel.[b]				High Temperature Storage[c]			
	0 Hours		Post Mechanical		Tested at 25°C		Tested at 125°C[d]	
	Z_3		Z_3		Z_3		Z_3	
DC-E2907-44-1 (NP[e])								
40527-516-8	46.32		2.930		5.590		257.4	
-9	34.79		2.930		40.22		279.1	
-16	42.21		2.920		5.120		111.9	
-69	80.03		2.720		5.120		112.8	
Avg. % Change (NP)	-		-94.3		-72.4		+1358	
DC-E2907-44-1 (WP[f])								
40527-516-4	26.54		3.120		7.040		329.4	
-12	26.82		3.680		6.220		268.4	
-21	25.70		2.870		5.040		113.3	
-30	25.89		2.860		5.080		115.0	
Avg % Change (WP)	-		-88.1		-77.7		+3533	
Avg % Change Overall	-		-91.2		-75.1		+2446	
3 to 1 Mixture (NP)								
40527-516-14	5.440		3.020		9.430		172.1	
-18	3.200		2.930		5.560		253.9	
-23	5.280		3.210		4.790		119.2	
-33	5.130		2.630		26.93		123.6	
Avg % Change (NP)	-		-38.0		+145.4		+1432	
3 to 1 Mixture (WP)								
40527-516-11	26.37		3.040		5.020		358.2	
-19	26.60		3.110		5.130		341.5	
-38	26.00		3.060		5.010		157.9	
-50	21.63		2.890		5.710		152.8	
Avg % Change (WP)	-		-88.0		-79.24		+4841	
Avg % Change Overall	-		-63.0		+33.1		+3137	
Uncoated Controls (NP)								
40527-516-17	63.19		-102.4[g]		-102.4[g]		322.4[g]	
-24	36.89		2.920		10.61		103.2	
-27	33.21		2.940		6.890		269.8	
-28	27.43		3.240		5.250		470.2	
-37	35.87		2.870		4.790		157.3	
-46	84.95		3.030		5.590		468.5	
-60	84.36		3.040		4.880		121.1	
-78	63.53		22.41		13.35		184.3	
Avg. % Change	-		-89.0		-86.0		+3455	

[a] Mechanical Shock: 1,500 g's, 5 shocks, Method 2002.1, Condition B, in Y_2 direction

[b] Constant Acceleration: 10,000 g's, Method 2001.1, Condition B, in Y_2 direction

[c] High Temperature Storage: 1,000 hours, 150°C, Method 1008.1, Condition C

[d] Percent change based on value measured at 25°C after storage.

[e] NP = No added particles

[f] WP = With added particles

[g] Failed device, not included in average % change at time failure occurred

TABLE 24. TEST DEVICES, APPLIED BIASES, PARAMETERS MEASURED AND SPECIFICATION REQUIREMENTS FOR HYBRID TEST CIRCUITS

Devices	Applied Bias	Parameters Measured	Specification Requirement
Pd/Ag/Pd oxide chip resistors	1 volt	Resistance	450 ohms $\pm$ 20%
NiCr thin film resistors	5 volts	Resistance	500K ohms $\pm$5%
JFETs, 2N4391	Drain: +20 volts Gate: -7.5 volts Source: ground	Zero gate voltage drain current (I_{DSS})	$\leq$150 mA
Mesa transistors, 2NC5975	Emitter & base: + 20 volts Collector: ground	Collector-emitter cutoff current (I_{CEX})	$\leq$1.0 mA
		DC current gain (h_{FE})	25 to 130
Operational amplifiers, LM741	Inputs: ground Supplies: +15 and -15 volts	Offset voltage (V_{IO})	5.0 mV max.
		Positive input bias current (I_B+)	$\leq$500 nA
		Negative input bias current (I_B-)	$\leq$500 nA
CMOS, CD4001	Collector supply voltage: + 5 volts Inputs: ground	Quiescent current (I_{DD})	<1.0 µA
Interdigitated thin film gold capacitor, 0.0635 mm (0.0025 in.) spacing	Not biased	Leakage current Breakdown voltage	- -

and package related. The coating may have sensitized the unpassivated resistors to reducing agents but a larger and more controlled sample would be required to determine this effect. The fact that many of the coated unpassivated thick film resistors decreased in resistance when measured at 125°C (Table 14), tends to support the fact that the coating is acting as a sensitizer. An attempt was made to measure the electrical parameters of the circuits at -55°C also, but the proper fixturing was not available for handling this particular package on the Tektronix 3260 tester. Moisture condensation on the test fixture resulted in inaccurate data.

In the case of the thin film NiCr resistors (Table 16 and 17), the coated and uncoated resistors showed identical changes within the accuracy of the Tektronix 3260 tester. The initial measurements for the coated circuits containing particles were made on a different day than the initial measurements on the other circuits. The initially measured values for the circuits with particles are believed to be about one percent lower than the actual values causing the average percent change measured after the mechanical shock and constant acceleration tests to be about one percent high. This is based on the fact that the average percent changes in resistances after the 1000 hour storage at 150°C ranged from +0.45 to 0.66% for the coated and uncoated passivated resistors and from +0.49 to 0.66% for the coated and uncoated unpassivated resistors. The changes in resistance values when measured at 25 and 125°C were also identical within the accuracy of the Tektronix 3260.

The results of the zero gate voltage drain current (I_{DSS}) measurements performed on the unpassivated and passivated 2N4391 JFETs are shown in Tables 18 and 19. All of the devices remained well within the specification requirements with no evidence of coating related problems. The changes in the passivated and unpassivated devices were also comparable indicating little or no mobile ion content in the coatings.

Offset voltage measurements performed on the LM741 op amps (Table 20) again showed no problems due to the coatings; all of the devices remained within the specification requirements. The average percent change in value in this case was calculated without regard to the sign (+ or -) of the voltage.

The results of the collector-emitter cutoff current (I_{CEX}) and gain (h_{FE}) measurements performed on the 2NC5975 mesa transistors are shown in Tables 21 and 22. No failures occurred in the coated circuits and the leakages decreased in most cases. All the devices remained well within the specification requirements. These transistors have unpassivated junctions and the low leakage currents again indicate that the mobile ion content of the coatings is very low.

Quiescent current (I_{DD}) measurements of the CD4001 CMOS (Table 23) devices also showed leakage currents well within the specification requirement of <1000 nA on completion of the tests. No failures occurred with the coated devices but one device in uncoated control circuit 40527-516-17 (Table 23) failed.

Each circuit package contained a total of 222 wire bonds distributed as shown in Table 25. A total of 1776 wire bonds per coating were therefore evaluated with no bond failures. In addition, all of the coated devices with the exception of the Pd/Ag/Ag oxide thick film resistors remained within the specification requirements. The resistance changes in the coated thick film resistors were comparable to the uncoated controls. The coating therefore did not serve as a barrier to the reducing contaminants present in the package ambient and may have increased the sensitivity of the unpassivated resistors to the contaminants.

3.3.3 Burn-In and Operating Life Test Results

A second set of hybrid test specimens, distributed as shown in Figure 3, were subjected to burn-in per MIL-STD-883B, Method 1015.2, Condition A, for 240 hours at 125°C followed by the operating life test per MIL-STD-883B, Method 1005.2, Condition A, 1000 hours at 125°C. The test devices, and biases applied, parameters measured, and specification requirements are given in Table 24.

3.3.3.1 Electrical Test Results

The results of the electrical tests on the hybrids are shown in Tables 26 through 35. The Pd/Ag/Pd oxide thick film resistors (Tables 26 and 27) showed resistance changes greater than those which occurred during the mechanical and high temperature storage tests (Tables 14 and 15) indicating

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SOLVENT REMOVABLE COATINGS FOR CONTAMINANT PROTECTION OF MICROC--ETC(U)
NOV 78 B L WEIGAND, J J LICARI, L R SCHULZ F33615-77-C-5141
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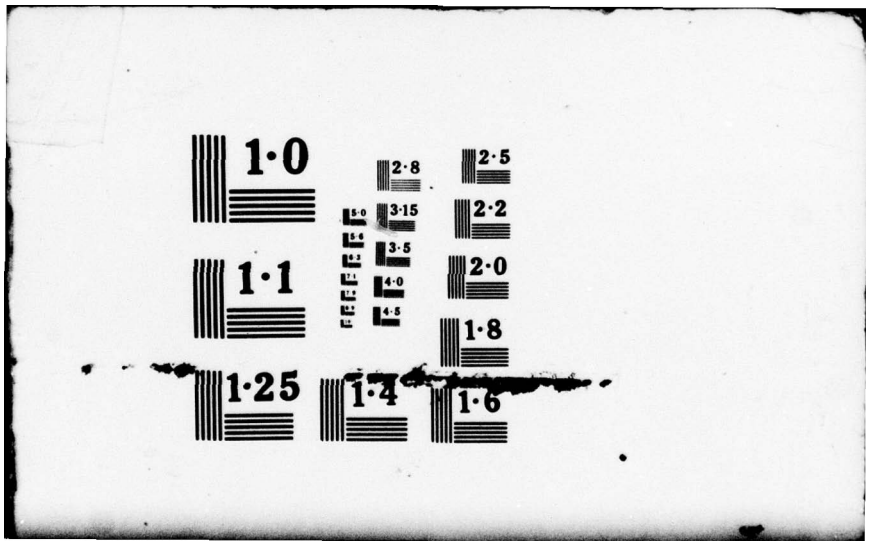
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TABLE 25. TYPE AND NUMBER OF WIRE BONDS CONTAINED IN CIRCUIT PACKAGES

Wire Type	Bonding Surface	Bonding Method	No. of Bonds/ Circuit Package	No. of Bonds/ Coating
1 mil aluminum	Thin film aluminum (device)	Ultrasonic wedge	40	320
1 mil aluminum	Thin film gold (substrate)	Ultrasonic wedge	40	320
1.5 mil gold	Thin film aluminum (mesa transistors)	Ultrasonic wedge	6	48
1.5 mil gold	Thick film gold (thick film resistors)	Ultrasonic wedge	8	64
1.5 mil gold	Thin film gold (substrate)	Thermocompression wedge	57	456
1.5 mil gold	Thin film gold (package posts)	Thermocompression wedge	57	456
1.5 mil gold	Thin film gold (substrate)	Ultrasonic wedge	14	112
		TOTALS	222	1776

TABLE 26. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR UNPASSIVATED Pd/Ag THICK FILM RESISTOR CHIPS

Coating/ Circuit No.	Resistance (Ohms)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	R_1	R_2	R_1	R_2	R_1	R_2	R_1	R_2	R_1	R_2
DC-E2907-44-1 (NP*)										
40527-516-15	441.5	437.7	419.5	426.5	367.5	354.7	279.7	237.6	131.0	106.0
-31	413.9	452.0	402.5	448.0	363.5	442.0	290.0	413.5	143.0	272.5
-40	440.5	479.5	431.0	438.5	354.5	333.5	212.0	186.0	68.0	54.2
-68	496.0	403.5	407.5	387.0	321.5	354.5	207.5	291.5	60.6	134.5
Avg. % Change (NP)	-		-5.73		-18.9		-40.6		-72.8	
DC-E2907-44-1 (WP*)										
40527-516-41	446.6	449.0	446.3	441.5	438.5	419.5	419.0	371.0	326.5	253.5
-44	475.0	454.1	470.0	442.0	451.5	411.5	423.3	365.0	337.0	259.0
-59	444.0	482.0	391.0	399.5	309.0	301.0	232.5	227.9	141.0	138.0
-74	435.5	438.0	425.5	328.1	348.0	160.0	204.5	61.62	80.5	16.9
Avg % Change (WP)	-		-7.73		-21.7		-40.9		-57.2	
Avg % Change Overall	-		-6.73		-20.3		-40.8		-65.0	
3 to 1 Mixture (NP)										
40527-516-36	436.5	458.0	396.0	401.0	364.5	319.5	262.6	170.0	80.0	33.4
-39	447.0	470.0	435.0	438.9	411.5	383.5	351.0	262.0	135.0	65.5
-45	447.5	464.0	441.5	418.5	414.5	329.5	308.0	156.5	101.5	40.5
-67	459.5	423.5	393.5	316.5	263.5	170.5	121.0	61.25	26.2	15.9
Avg % Change (NP)	-		-10.1		-26.3		-53.1		-86.2	
3 to 1 Mixture (WP)										
40527-516-55	451.0	442.8	433.0	440.5	382.0	414.5	308.6	286.5	83.0	67.5
-61	433.5	433.0	431.3	433.0	418.0	420.5	388.0	388.0	343.0	331.5
-70	460.7	459.5	456.5	458.7	437.0	449.2	417.5	423.5	343.5	374.0
-75	439.6	426.0	428.5	426.0	391.0	419.5	342.5	409.5	225.5	384.5
Avg % Change (WP)	-		-1.09		-6.05		-16.4		-39.3	
Avg % Change Overall	-		-5.60		-16.8		-34.8		-62.8	
Uncoated Controls (NP)										
40527-516-20	446.2	469.5	417.5	414.0	369.0	308.5	292.0	190.0	180.0	105.5
-22	449.0	455.9	387.5	399.5	274.0	292.5	143.0	131.5	64.8	52.5
-26	420.0	453.0	405.5	443.5	387.0	403.5	327.5	319.0	223.0	208.5
-32	439.9	466.0	438.0	427.5	440.0	410.5	441.5	383.0	449.5	344.0
-34	490.5	446.2	434.0	434.0	409.0	422.5	372.0	402.0	288.0	356.5
-42	454.0	435.5	430.5	350.0	411.5	308.0	382.6	252.4	266.5	129.0
-57	436.5	426.0	324.0	406.9	258.0	339.0	179.0	218.5	90.5	105.5
-79	483.8	484.0	457.0	353.0	399.5	220.0	285.6	96.5	143.0	40.4
Avg. % Change	-		-10.1		-22.1		-39.1		-58.0	

*(NP) = No added particles
(WP) = With added particles

TABLE 27. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR PASSIVATED Pd/Ag THICK FILM RESISTOR CHIPS

Coating/ Circuit No.	Resistance (Ohms)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	R_3	R_4	R_3	R_4	R_3	R_4	R_3	R_4	R_3	R_4
DC-E2907-44-1 (NP*)										
40527-516-15	417.0	444.0	414.5	432.5	414.0	416.0	410.5	395.0	401.5	361.0
-31	410.5	411.0	408.0	408.1	409.5	406.5	408.5	402.5	406.0	390.3
-40	424.5	424.1	419.5	422.5	413.0	423.5	392.5	421.0	369.0	413.5
-68	409.1	425.5	400.0	417.0	388.0	400.0	369.5	363.0	318.5	286.0
Avg. % Change (NP)	-		-1.31		-2.84		-6.05		-12.5	
DC-E2907-44-1 (WP*)										
40527-516-41	448.5	418.5	448.0	418.0	450.0	419.5	449.0	419.5	447.0	419.5
-44	411.0	423.5	410.0	423.0	411.6	424.9	411.5	423.5	411.0	413.0
-59	397.0	397.0	396.5	354.0	397.0	312.0	394.5	280.5	391.0	246.9
-74	414.5	427.9	395.5	415.0	382.5	396.0	368.4	373.5	338.0	330.5
Avg % Change (WP)	-		-2.33		-4.33		-6.52		-10.2	
Avg % Change Overall	-		-1.82		-3.59		-6.29		-11.4	
3 to 1 Mixture (NP)										
40527-516-36	433.0	425.0	431.0	420.0	430.5	418.0	427.0	412.0	418.7	401.5
-39	427.4	412.1	425.0	408.0	425.5	404.0	422.5	396.0	414.0	366.5
-45	434.1	405.5	414.3	389.5	387.5	379.0	364.0	363.5	321.0	328.0
-67	442.5	448.5	424.5	381.7	396.0	309.5	344.0	245.0	268.5	120.0
Avg % Change (NP)	-		-3.91		-8.11		-13.2		-23.0	
3 to 1 Mixture (WP)										
40527-516-55	445.6	410.0	416.0	409.3	375.0	407.9	331.5	400.5	220.5	380.5
-61	444.5	426.5	444.5	426.0	446.5	424.4	446.0	406.9	442.0	374.0
-70	404.5	424.5	403.5	424.0	400.0	422.5	391.5	413.7	380.0	396.1
-75	405.0	421.0	405.0	415.5	405.0	396.5	395.0	370.0	379.5	315.5
Avg % Change (WP)	-		-1.12		-3.07		-6.70		-14.6	
Avg % Change Overall	-		-2.52		-5.59		-9.95		-18.8	
Uncoated Controls (NP)										
40527-516-20	415.0	424.0	395.5	406.5	384.0	396.5	370.0	386.3	347.5	357.5
-22	446.7	410.5	424.3	408.0	411.5	409.5	397.5	409.5	379.0	409.5
-26	425.4	426.0	342.0	390.0	310.0	372.5	281.0	355.0	238.0	336.0
-32	426.0	421.5	406.5	415.5	399.5	411.5	387.7	401.0	362.6	382.0
-34	387.0	411.0	355.0	406.4	339.0	404.9	317.5	399.0	261.0	379.8
-42	411.0	442.6	404.5	439.9	397.5	440.5	384.2	437.5	357.5	429.5
-57	423.0	410.5	354.0	400.2	310.5	395.5	269.0	390.0	218.0	376.5
-79	423.2	420.5	354.6	352.5	316.9	323.0	282.7	286.0	236.5	241.0
Avg. % Change	-		-6.97		-10.4		-14.4		-21.0	

*(NP) = No added particles
(WP) = With added particles

TABLE 28. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR PASSIVATED NiCr THIN FILM RESISTOR CHIPS

Coating/ Circuit No.	Resistance (K ohms)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	R_5	R_6	R_5	R_6	R_5	R_6	R_5	R_6	R_5	R_6
DC-E2907-44-1 (NP*)										
40527-516-15	496.8	496.5	494.9	494.9	497.0	497.0	497.3	497.0	497.4	497.5
-31	497.0	-	494.9	-	497.0	-	497.4	-	497.5	-
-40	496.5	496.5	495.0	495.5	497.0	497.5	497.5	497.5	497.5	497.5
-68	496.5	496.5	494.9	495.0	497.0	497.0	497.2	497.1	497.5	497.0
Avg. % Change (NP)	-		-0.32		+0.092		+0.14		+0.16	
DC-E2907-44-1 (WP*)										
40527-516-41	491.0	490.9	494.5	494.8	497.0	497.0	497.1	497.0	497.4	497.1
-44	490.9	491.0	494.5	494.5	496.6	496.8	497.0	497.0	497.0	497.0
-59	493.0	490.9	496.8	494.6	498.9	496.8	499.0	497.0	499.1	497.0
-74	491.9	490.5	495.5	494.8	497.5	497.0	497.8	497.0	497.9	497.3
Avg % Change (WP)	-		+0.76		+1.21		+1,24		+1.26	
Avg % Change Overall	-		+0.22		+0.65		+0.69		+0.71	
3 to 1 Mixture (NP)										
40527-516-36	497.0	500.0	494.8	497.5	496.9	499.5	497.0	500.0	497.4	500.0
-39	497.0	497.5	494.5	495.0	496.6	497.0	497.0	497.5	497.0	497.5
-45	497.0	497.4	494.8	495.0	497.0	497.1	497.2	497.5	497.5	497.5
-67	497.0	497.5	494.9	495.0	497.0	497.5	497.3	497.5	497.5	497.5
Avg % Change (NP)	-		-0.47		-0.045		+0.015		+0.038	
3 to 1 Mixture (WP)										
40527-516-55	490.8	491.3	494.5	495.0	496.6	497.0	497.0	497.5	497.0	497.5
-61	491.0	492.0	494.4	495.5	496.5	497.5	496.9	497.5	496.9	497.6
-70	490.9	491.0	494.4	494.5	496.5	496.5	496.8	497.0	497.0	497.0
-75	491.0	490.5	494.5	494.5	496.5	496.5	496.9	496.8	496.9	496.6
Avg % Change (WP)	-		+0.73		+1.15		+1.22		+1.22	
Avg % Change Overall	-		+0.13		+0.55		+0.62		+0.63	
Uncoated Controls (NP)										
40527-516-20	496.5	496.5	494.9	494.8	497.0	497.0	497.0	497.5	497.4	497.5
-22	496.5	496.5	494.9	495.0	497.0	497.0	497.2	497.2	497.4	497.5
-26	496.5	496.5	494.6	494.8	496.9	497.0	497.0	497.0	497.1	497.1
-32	496.8	496.6	494.5	494.5	496.8	496.9	497.0	497.0	497.0	497.0
-34	496.4	496.5	494.5	494.5	496.8	496.9	497.0	497.0	497.0	497.2
-42	496.2	498.4	494.8	497.0	497.0	499.0	497.4	499.4	497.5	499.5
-57	497.0	497.9	495.5	496.1	497.5	498.3	498.0	498.5	498.0	497.5
-79	498.0	497.0	496.0	495.0	498.0	497.0	498.5	497.5	498.5	497.5
Avg. % Change	-		-0.36		+0.08		+0.13		+0.14	

*(NP) = No added particles
(WP) = With added particles

TABLE 29. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR UNPASSIVATED NiCr THIN FILM RESISTOR CHIPS

Coating/ Circuit No.	Resistance (K ohms)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	R_7	R_8	R_7	R_8	R_7	R_8	R_7	R_8	R_7	R_8
DC-E2907-44-1 (NP*)										
40527-516-15	486.5	491.5	485.5	490.5	488.0	492.5	488.1	492.9	488.0	493.0
-31	478.5	474.0	477.5	473.0	479.6	475.0	480.0	475.4	480.0	475.4
-40	522.2	484.5	521.4	483.4	523.5	485.5	524.0	485.7	523.5	485.5
-68	336.3	502.4	336.1	501.0	338.4	503.5	338.7	503.5	339.1	503.5
Avg. % Change (NP)	-		-0.20		+0.27		+0.33		+0.36	
DC-E2907-44-1 (WP*)										
40527-516-41	478.4	455.5	482.5	458.3	487.4	460.5	485.0	460.9	485.0	460.9
-44	480.0	514.5	484.0	517.5	486.4	520.0	486.5	520.0	486.5	520.0
-59	478.0	476.5	482.5	479.5	484.5	481.6	485.0	482.0	484.7	482.0
-74	342.6	492.5	344.0	495.9	344.9	498.0	345.8	498.0	356.5	498.2
Avg % Change (WP)	-		+0.70		+1.22		+1.22		+1.23	
Avg % Change Overall	-		+0.25		+0.75		+0.78		+0.80	
3 to 1 Mixture (NP)										
40527-516-36	500.5	498.5	499.0	496.5	501.5	499.0	501.5	499.0	501.5	499.1
-39	488.2	480.0	486.5	478.0	488.8	480.5	489.0	480.5	489.0	480.5
-45	485.0	486.0	483.5	484.5	486.0	486.5	486.0	487.0	486.0	487.0
-67	519.0	501.0	517.1	499.0	519.5	501.1	520.0	501.5	520.0	501.5
Avg % Change (NP)	-		-0.36		+0.12		+0.16		+0.16	
3 to 1 Mixture (WP)										
40527-516-55	478.3	507.5	482.5	511.4	484.9	513.5	485.0	513.5	485.0	513.8
-61	480.6	483.6	484.5	486.5	487.0	488.5	487.1	489.0	487.0	489.0
-70	474.1	479.5	478.0	482.5	480.5	484.5	480.7	484.8	480.5	484.5
-75	480.0	507.0	484.0	510.0	486.5	512.0	486.5	512.5	486.5	512.4
Avg % Change (WP)	-		+0.74		+1.20		+1.25		+1.25	
Avg % Change Overall	-		+0.19		+0.66		+0.71		+0.71	
Uncoated Controls (NP)										
40527-516-20	517.5	486.5	516.0	485.0	518.5	487.5	518.5	487.9	518.5	488.0
-22	480.1	430.0	479.0	428.6	481.0	431.4	481.5	431.6	481.3	431.1
-26	475.5	478.5	474.1	477.5	476.5	479.5	476.5	480.0	476.5	480.0
-32	474.0	484.5	472.2	485.6	474.5	488.3	475.0	489.0	474.5	489.5
-34	478.5	484.0	477.0	483.0	479.4	485.0	479.5	485.3	479.5	485.5
-42	482.0	490.0	480.5	488.9	483.0	491.0	483.5	491.4	483.5	491.5
-57	337.5	481.5	336.0	480.5	338.0	482.5	338.5	483.0	338.5	482.5
-79	478.5	480.0	476.5	478.5	479.0	480.0	479.0	481.0	479.5	481.1
Avg. % Change	-		-0.26		+0.23		+0.30		+0.30	

*(NP) = No added particles
(WP) = With added particles

TABLE 30. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR UNPASSIVATED 2N4391 JFET's, ZERO GATE VOLTAGE DRAIN CURRENT

Coating/ Circuit No.	I_{DSS} (ma)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	Q_3	Q_4	Q_3	Q_4	Q_3	Q_4	Q_3	Q_4	Q_3	Q_4
DC-E2907-44-1 (NP*)										
40527-516-15	99.5	99.8	96.3	96.8	99.6	100.3	98.9	99.5	98.9	99.8
-31	89.7	106.6	85.7	102.7	89.2	106.1	88.4	105.3	88.3	105.2
-40	87.2	82.9	83.8	79.8	86.9	82.9	86.2	82.3	86.3	82.3
-68	89.7	72.8	86.0	69.5	89.3	72.8	88.3	72.1	88.5	72.3
Avg. % Change (NP)	-		-3.79		-0.15		-0.99		-0.92	
DC-E2907-44-1 (WP*)										
40527-516-41	97.6	101.6	97.0	101.2	100.4	104.5	99.4	103.5	99.4	103.4
-44	99.6	89.6	99.6	89.8	103.4	93.3	102.8	92.7	102.5	92.3
-59	89.8	89.4	89.0	88.9	92.4	92.2	91.8	91.9	91.8	92.0
-74	66.0	62.8	65.4	62.4	68.3	65.3	68.0	64.9	68.1	65.1
Avg % Change (WP)	-		-0.45		+3.36		+2.67		+2.61	
Avg % Change Overall	-		-2.12		+1.61		+0.84		+0.85	
3 to 1 Mixture (NP)										
40527-516-36	66.6	103.4	65.0	101.5	68.4	104.9	67.8	104.4	67.9	104.3
-39	78.1	76.8	76.9	75.4	79.8	78.8	79.2	78.3	79.5	78.4
-45	96.3	95.3	95.0	94.1	98.4	97.5	97.9	96.8	97.5	96.5
-67	97.8	99.0	95.7	97.0	99.5	100.7	98.3	99.5	98.9	100.1
Avg % Change (NP)	-		-1.78		+2.06		+1.25		+1.44	
3 to 1 Mixture (WP)										
40527-516-55	103.9	86.3	103.7	86.2	106.6	89.3	105.9	88.7	105.9	88.7
-61	70.3	63.8	69.7	63.3	73.2	66.7	72.7	66.1	72.7	66.3
-70	100.3	67.9	100.0	67.9	103.5	71.3	102.9	70.8	102.9	70.8
-75	103.4	84.3	102.8	83.8	106.4	87.3	105.6	86.7	105.8	86.7
Avg % Change (WP)	-		-0.41		+3.54		+2.82		+2.88	
Avg % Change Overall	-		-1.10		+2.80		+2.04		+2.16	
Uncoated Controls (NP)										
40527-516-20	81.0	67.9	77.2	64.7	81.0	68.3	80.3	67.6	80.5	67.8
-22	81.7	82.3	78.2	79.0	81.7	82.4	81.2	82.0	81.2	81.9
-26	100.4	62.5	96.8	59.1	100.4	62.6	99.5	62.1	99.7	62.0
-32	92.7	76.3	89.3	73.2	92.7	76.7	92.2	76.3	92.3	76.5
-34	107.0	88.2	103.4	84.8	107.0	88.4	106.2	87.7	106.4	87.7
-42	100.3	104.7	96.9	101.7	100.4	105.0	99.4	104.0	99.7	104.2
-57	78.2	83.1	75.2	79.8	78.8	83.7	77.8	82.7	78.3	83.1
-79	90.6	100.8	86.7	97.3	90.2	100.8	89.5	100.3	89.2	100.2
Avg. % Change	-		-3.89		+0.17		-0.64		-0.50	

*(NP) = No added particles
(WP) = Added particles

TABLE 31. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR PASSIVATED 2N4391 JFETs, ZERO GATE VOLTAGE DRAIN CURRENT

Coating/ Circuit No.	I_{DSS} (ma)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	Q_5	Q_6	Q_5	Q_6	Q_5	Q_6	Q_5	Q_6	Q_5	Q_6
DC-E2907-44-1 (NP*)										
40527-516-15	60.7	40.6	57.7	37.6	61.2	41.1	60.5	40.6	60.7	40.6
-31	64.3	73.5	60.8	69.8	64.2	73.3	63.8	72.7	63.5	72.6
-40	64.7	65.4	61.7	62.4	64.9	65.4	64.5	65.0	64.4	65.1
-68	63.6	43.2	60.3	40.1	63.8	43.6	62.9	43.0	63.0	43.1
Avg. % Change (NP)	-		-5.38		+0.032		-0.63		-0.63	
DC-E2907-44-1 (MP*)										
40527-516-41	66.2	58.3	65.8	58.2	69.2	61.5	68.4	60.7	68.4	60.7
-44	62.6	65.9	62.7	66.2	66.2	69.8	65.9	69.2	65.5	69.1
-59	61.7	55.8	61.2	55.3	64.5	58.8	64.2	58.3	64.2	58.3
-74	75.2	91.7	74.7	91.1	77.7	93.7	77.2	93.2	77.3	93.0
Avg % Change (MP)	-		-0.41		+4.47		+3.67		+3.55	
Avg % Change Overall	-		-2.90		+2.25		+1.52		+1.46	
3 to 1 Mixture (NP)										
40527-516-36	41.1	62.0	39.6	60.5	43.1	63.9	42.6	63.5	42.6	63.5
-39	55.1	51.1	53.9	50.0	57.3	53.3	56.8	52.8	57.2	53.1
-45	61.4	60.0	60.1	58.8	63.7	62.2	63.0	61.6	62.8	61.5
-67	42.7	39.6	41.3	38.2	44.9	41.80	44.1	41.3	44.6	41.5
Avg % Change (NP)	-		-2.57		+4.16		+3.03		+3.34	
3 to 1 Mixture (MP)										
40527-516-55	60.2	57.2	60.1	57.3	63.3	60.3	62.8	59.8	62.9	59.8
-61	66.3	40.9	65.9	40.6	69.3	44.0	68.7	43.6	68.7	43.6
-70	67.1	62.7	67.2	62.8	70.5	66.0	70.0	65.5	70.0	65.6
-75	65.6	65.0	65.4	64.8	68.9	68.3	68.1	67.5	68.1	67.6
Avg % Change (MP)	-		-0.19		+5.28		+4.15		+4.39	
Avg % Change Overall	-		-1.38		+4.72		+3.59		+3.87	
Uncoated Controls (NP)										
40527-516-20	74.6	82.2	71.3	78.7	74.9	82.5	74.3	81.9	74.3	81.9
-22	58.4	61.5	55.4	58.5	58.8	62.0	58.4	61.5	58.3	61.3
-26	53.6	66.4	50.5	63.3	53.9	66.7	53.6	66.2	53.5	66.1
-32	42.6	89.0	39.6	85.8	43.0	89.3	42.6	88.8	42.7	88.8
-34	62.6	79.6	59.5	76.4	63.1	80.1	62.5	79.2	62.2	79.2
-42	57.9	40.4	54.8	37.6	58.2	41.1	57.4	40.3	57.8	40.7
-57	53.5	54.6	50.8	51.9	54.3	55.4	53.5	58.6	53.9	55.1
-79	64.8	62.5	61.5	59.2	64.9	62.7	64.5	62.5	64.5	62.5
Avg. % Change	-		-4.92		+0.67		+0.16		+0.16	

*(NP) = No added particles
(MP) = With added particles

TABLE 32. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR LM741 OP AMPS, OFFSET VOLTAGE

Coating/ Circuit No.	Offset Voltage (mv)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	Z_1	Z_2	Z_1	Z_2	Z_1	Z_2	Z_1	Z_2	Z_1	Z_2
DC-E2907-44-1 (NP*)										
40527-516-15	1.848	1.091	-12.88[a]	-13.18[a]	-12.68[a]	-12.98[a]	-12.68[a]	-12.98[a]	-12.68[a]	-12.98[a]
-31	1.795	0.3534	2.121	0.5962	1.916	0.4230	1.929	0.5306	2.058	0.4072
-40	0.8451	2.086	1.248	2.557	1.216	2.327	1.215	2.430	1.146	2.380
-68	0.6122	4.655	0.8061	4.551	0.8341	4.575	0.8201	4.693	0.7952	4.692
Avg. % Change (NP)	-		+14.8[a]		+9.12[a]		+12.4[a]		+10.9[a]	
DC-E2907-44-1 (WP*)										
40527-516-41	2.524	-0.0009	2.565	-0.0008	2.581	-0.0004	2.725	-0.0004	2.607	-0.0005
-44	1.243	2.162	1.281	2.225	1.017	1.898	1.283	2.028	1.251	1.986
-59	2.008	0.7232	1.970	0.6757	2.111	0.6583	2.204	0.6906	2.073	0.6813
-74	0.3009	1.594	0.4077	1.466	0.3570	1.524	0.3702	1.581	0.3364	1.620
Avg % Change (WP)	-		+0.33		-3.88		+3.09		-0.01	
Avg % Change Overall	-		+7.57		+2.62		+7.70		+5.45	
3 to 1 Mixture (NP)										
40527-516-36	3.053	1.909	3.108	1.836	3.071	1.883	3.047	1.779	2.974	1.768
-39	-2.404	2.312	-2.312	2.406	-2.114	2.592	-2.191	2.563	-2.257	2.548
-45	3.726	-1.085	3.874	-1.051	3.784	-0.9740	3.929	-0.9400	-12.84[a]	-13.08[a]
-67	1.692	1.903	1.870	2.049	1.807	1.854	1.855	1.904	1.757	1.970
Avg % Change (NP)	-		+2.33		-0.028		+0.69		+0.01	
3 to 1 Mixture (WP)										
40527-516-55	2.263	0.7842	2.503	0.8321	2.481	1.016	2.482	1.056	2.403	0.7952
-61	1.090	1.448	1.374	1.565	1.278	1.594	2.463	1.629	12.40[a]	1.504
-70	1.318	0.9790	1.159	0.7262	1.315	0.9740	1.255	0.7442	1.263	0.8911
-75	2.684	3.021	2.839	3.130	2.585	2.845	2.737	3.073	2.718	2.986
Avg % Change (WP)	-		+3.98		+3.69		+13.6		+0.50	
Avg % Change Overall	-		+3.16		+1.86		+7.15		+0.26	
Uncoated Controls (NP)										
40527-516-20	0.7542	3.232	0.8091	3.528	0.8961	3.388	0.9910	3.569	0.8961	3.353
-22	2.918	1.329	3.146	1.444	-12.73[a]	1.616	-13.14[a]	-12.63[a]	-13.15[a]	-12.64[a]
-26	1.823	1.011	2.096	1.205	1.955	1.364	2.120	1.241	1.852	1.180
-32	2.087	1.267	2.076	1.388	2.271	1.593	2.340	1.605	2.197	1.517
-34	0.5582	4.426	0.8391	4.358	-13.04[a]	-13.03[a]	-13.08[a]	-13.03[a]	-13.08[a]	-13.06[a]
-42	1.048	1.157	1.290	1.334	1.036	1.029	1.318	1.368	1.240	1.180
-57	2.749	-1.543	3.084	-1.087	3.075	-1.051	3.020	-1.321	2.966	-1.361
-79	0.7262	1.211	1.105	1.533	0.7962	1.359	0.9470	1.508	1.050	1.474
Avg. % Change	-		+8.92		+7.48[a]		+16.0[a]		+8.91[a]	

*(NP) = No added particles
(WP) = With added particles

[a]Failed device, not included in average % change at time failure occurred

TABLE 33. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR 2NC5975 MESA TRANSISTORS, COLLECTOR-EMITTER CUTOFF CURRENT

Coating/ Circuit No.	I_{CEX} (mA)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
DC-E2907-44-1 (NP*)										
40527-516-15	0.0035	0.0004	0.0002	0.0001	0.0001	0.0001	0.0002	0.0001	0.0004	0.0001
-31	0.0039	0.0007	0.0002	0.0002	0.0001	0.0002	0.0001	0.0002	0.0002	0.0001
-40	0.0772	0.0007	0.0049	0.0018	0.0042	0.0012	0.0043	0.0014	0.0044	0.0016
-68	0.0006	0.2300	0.0002	0.1978	0.1998	0.2027	0.0002	0.2064	0.0004	0.2053
Avg. % Change (NP)	-		-35.2		+28.8		-33.3		-33.0	
DC-E2907-44 1 (WP*)										
40527-516-41	0.0036	0.0332	0.0006	0.0033	0.0004	0.0031	0.0006	0.0037	0.0006	0.0044
-44	0.0141	0.0008	0.0035	0.0001	0.0002	0.0001	0.0056	0.0001	0.0073	0.0001
-59	0.0018	0.0031	0.0006	0.0015	0.0004	0.0012	0.0004	0.0013	0.0008	0.0017
-74	0.0006	0.0010	0.0002	0.0005	0.0001	0.0005	0.0001	0.0006	0.0004	0.0008
Avg % Change (WP)	-		-82.3		-89.7		-78.7		-72.3	
Avg % Change Overall	-		-58.8		-30.5		-56.0		-52.7	
3 to 1 Mixture (NP)										
40527-516-36	0.0006	0.0003	0.0003	0.0003	0.0001	0.0002	0.0002	0.0002	0.0002	0.0004
-39	0.3658	0.0009	0.1590	0.0008	0.1523	0.0006	0.1845	0.0001	0.1353	0.0008
-45	0.0034	0.0018	0.0043	0.0003	0.0039	0.0003	0.0054	0.0002	0.0076	0.0003
-67	0.0014	0.0001	0.0016	0.0001	0.0012	0.0001	0.0014	0.0001	0.0021	0.0001
Avg % Change (NP)	-		-55.5		-57.6		-48.7		-60.8	
3 to 1 Mixture (WP)										
40527-516-55	0.0077	0.0010	0.0012	0.0001	0.0010	0.0001	0.0011	0.0001	0.0014	0.0001
-61	0.0129	0.5503	0.0039	0.7525	0.0045	0.6498	0.0041	0.6106	0.0099	0.5637
-70	0.0011	0.0067	0.0003	0.0009	0.0001	0.0006	0.0002	0.0007	0.0004	0.0007
-75	0.0009	0.0008	0.0004	0.0001	0.0003	0.0001	0.0004	0.0001	0.0005	0.0001
Avg % Change (WP)	-		+30.6		+12.9		+6.17		-0.79	
Avg % Change Overall	-		-12.5		-22.4		-21.3		-30.8	
Uncoated Controls (NP)										
40527-516-20	0.0005	0.0005	0.0002	0.0001	0.0001	0.0001	0.0002	0.0001	0.0004	0.0001
-22	0.0034	0.0228	0.0002	0.0023	0.0001	0.0016	0.0002	0.0012	0.0004	0.0009
-26	0.0032	0.0007	0.0002	0.0001	0.0001	0.0001	0.0001	0.0003	0.0002	0.0002
-32	0.0001	0.0004	0.0010	0.0001	0.0013	0.0001	0.0022	0.0001	0.0038	0.0002
-34	0.0008	0.0026	0.0001	0.3844	0.0001	0.4663	0.0001	0.0037	0.0004	0.4187
-42	0.0033	-	0.0007	-	0.0005	-	0.0005	-	0.0008	-
-57	0.7132	0.7604	1.220[a]	0.9920	0.6340	0.0001	1.463[a]	0.9446	1.923[a]	0.9683
-79	0.0028	0.0015	0.0003	0.0004	0.0001	0.0002	0.0001	0.0002	0.0004	0.0002
Avg % Change	-		+71.6[a]		-27.1		+18.8[a]		+73.7[a]	

*(NP) = No added particles
(WP) = With added particles

[a]Failed device (leakage >1.0 ma), not included in average % change at time failure occurred

TABLE 34. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR 2NC5975 MESA TRANSISTORS, DC CURRENT GAIN

Coating/ Circuit No.	h_{FE}									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2	Q_1	Q_2
DC-E2907-44-1 (NP*)										
40527-516-15	119.8	124.0	119.7	123.9	119.0	123.2	118.7	122.8	117.8	122.6
-31	129.5	129.4	129.6	129.5	128.6	128.5	128.4	128.4	128.3	128.2
-40	110.2	128.3	109.8	127.1	109.2	125.2	109.7	123.7	109.3	119.1
-68	130.6	132.8	129.9	131.7	128.7	130.0	128.1	129.1	127.1	126.3
Avg. % Change (NP)	-		-0.34		-1.21		-1.63		-2.42	
DC-E2907-44-1 (WP*)										
40527-516-41	123.2	131.9	122.5	131.3	121.6	130.4	121.3	130.1	120.8	129.7
-44	121.1	121.4	120.9	121.4	120.4	120.7	120.3	122.1	120.0	121.9
-59	122.4	122.2	120.9	121.9	121.6	120.1	120.0	121.3	121.3	121.0
-74	125.4	127.2	125.3	126.9	124.4	126.2	124.3	125.9	124.2	125.7
Avg % Change (WP)	-		-0.37		-0.94		-0.99		-1.03	
Avg % Change Overall	-		-0.36		-1.08		-1.31		-1.73	
3 to 1 Mixture (NP)										
40527-516-36	131.6	126.8	131.5	126.8	130.4	126.0	130.1	125.8	129.4	125.5
-39	112.0	126.0	111.9	123.3	111.4	122.4	111.3	120.8	111.1	120.7
-45	126.0	125.1	125.9	124.2	125.1	123.1	124.7	122.3	123.9	122.0
-67	125.8	129.9	125.4	126.0	124.3	123.3	123.8	123.1	123.0	122.4
Avg % Change (NP)	-		-0.82		-1.71		-2.12		-2.51	
3 to 1 Mixture (WP)										
40527-516-55	124.4	129.8	124.2	129.4	123.5	128.7	123.4	128.5	122.2	123.7
-61	126.4	128.5	125.3	128.2	124.4	127.3	124.2	127.3	123.8	127.1
-70	127.3	125.1	126.1	124.2	124.5	123.1	123.1	128.1	121.6	126.1
-75	127.6	129.0	126.7	128.3	125.6	127.3	124.9	126.9	123.5	126.0
Avg % Change (WP)	-		-0.56		-1.34		-1.15		-2.37	
Avg % Change Overall	-		-0.69		-1.53		-1.64		-2.44	
Uncoated Controls (NP)										
40527-516-20	129.6	126.3	129.5	126.3	128.7	125.6	128.6	125.4	128.3	125.1
-22	129.3	119.5	129.4	118.9	128.6	118.2	128.5	117.2	128.4	118.2
-26	128.5	128.0	128.7	128.1	127.5	127.4	126.8	126.7	126.2	126.8
-32	126.3	128.3	126.1	128.2	125.3	127.5	125.1	127.4	124.9	127.4
-34	126.1	130.8	126.1	130.9	125.4	130.2	125.3	129.9	122.7	123.7
-42	121.0	126.7	120.9	126.7	120.4	126.0	120.3	125.9	122.9	125.7
-57	132.7	128.5	132.8	128.7	132.0	127.6	132.1	127.7	132.0	127.4
-79	125.7	132.7	125.8	132.8	125.0	132.0	124.9	132.0	124.8	131.9
Avg. % Change	-		-0.05		-0.62		-0.79		-1.16	

*(NP) = No added particles
(WP) = With added particles

TABLE 35. BURN-IN AND STEADY STATE LIFE TEST RESULTS FOR 4001 CMOS, QUIESCENT CURRENT

Coating/ Circuit No.	I_L (nA)									
	Burn-In (125°C)				Steady State Life (125°C)					
	0 Hours		240 Hours		168 Hours		500 Hours		1000 Hours	
	Z_3		Z_3		Z_3		Z_3		Z_3	
DC-E2907-44-1 (NP*)										
40527-516 -15	47.14		4.06		2.90		2.88		5.07	
-31	25.89		3.73		2.83		2.80		8.48	
-40	59.73		3.60		2.76		2.62		5.11	
-68	77.08		4.15		3.16		3.42		6.01	
Avg. % Change (NP)	-		-92.6		-94.4		-94.4		-88.2	
DC-E2907-44-1 (WP*)										
40527-516 -41	22.41		4.03		2.70		2.66		6.20	
-44	26.34		4.42		3.42		3.54		6.34	
-59	26.78		3.84		2.91		2.78		5.12	
-74	15.82		3.75		2.88		2.77		5.06	
Avg % Change (WP)	-		-82.4		-87.0		-87.1		-75.1	
Avg % Change Overall	-		-87.5		-90.7		-90.8		-81.7	
3 to 1 Mixture (NP)										
40527-516 -36	5.09		3.64		2.82		2.85		7.67	
-39	5.07		3.59		2.77		2.65		5.39	
-45	5.28		3.56		2.70		2.74		6.75	
-67	5.24		3.61		2.74		2.96		5.21	
Avg % Change (NP)	-		-30.4		-46.7		-45.8		+21.0	
3 to 1 Mixture (WP)										
40527-516 -55	26.38		3.66		2.69		2.72		6.55	
-61	25.73		3.96		2.68		2.75		9.05	
-70	25.66		3.74		2.74		2.65		4.76	
-75	24.24		3.95		2.66		2.77		4.82	
Avg % Change (WP)	-		-86.7		-81.5		-89.0		-75.3	
Avg % Change Overall	-		-58.6		-68.1		-67.4		-27.2	
Uncoated Controls (NP)										
40527-516-20	44.84		3.76		2.76		2.80		5.66	
-22	61.98		3.66		2.84		2.78		5.27	
-26	20.19		3.86		2.94		2.85		6.15	
-32	29.02		3.92		2.86		2.96		11.65	
-34	50.40		3.82		2.65		2.64		4.62	
-42	75.63		3.93		2.81		2.67		5.65	
-57	64.83		3.92		2.80		2.94		10.07	
-79	43.32		3.88		2.87		2.61		5.34	
Avg. % Change	-		-92.1		-94.2		-94.3		-86.1	

*(NP) = No added particles
(WP) = With added particles

that the applied bias was an accelerating factor. The passivated resistors again showed the lesser change. The resistance changes also appear to be device/package related rather than coating related as in the prior tests.

The coated and uncoated nichrome resistors (Tables 28 and 29) again showed identical changes within the accuracy of the Tektronix 3260. The circuits were initially tested on the same days as the circuits used in the mechanical and high temperature storage tests. The initially measured values for the coated circuits with particles are again believed to be about one percent lower than the actual values. In this case, the average resistance changes during the 1000 hour steady state life test ranged from +0.48 to 0.51% for the coated and uncoated passivated resistors and from +0.51 to 0.56% for the coated and uncoated unpassivated resistors. The changes in the coated and uncoated resistors, whether passivated or unpassivated, were therefore essentially identical.

Zero gate voltage drain current measurements (I_{DSS}) performed on the JFETs (Tables 30 and 31) again showed no failures and no evidence of coating-related problems on either the passivated or unpassivated devices.

The results of the offset voltage measurements performed on the LM741 op amps are shown in Table 32. Both devices in circuit 40527-516-15 coated with DC-E2907-44-1 failed, both devices in circuit 40527-516-45 and one device in circuit 40527-516-61 coated with the 3:1 coating formulation failed, and both devices in control circuits 40527-516-22 and -34 also failed. Failures in all of the circuits with the exception of 40527-516-61 were due to electrical overstresses during testing causing fusing of the leads to the positive supplies of the op amps. In the case of circuit 40527-516-61, the failure mode was not determined but was probably due to a similar electrical overstress. The average changes in offset voltages for the remainder of the coated op amps remained within the specification limits and were comparable to or less than the changes shown by the uncoated controls.

The results of the collector-emitter cutoff current (I_{CEX}) and gain (h_{FE}) measurements performed on the 2NC5975 mesa transistors are shown in Tables 33 and 34. No failures occurred in the coated circuits and the leakages decreased in most cases. The changes in gain were also well within

acceptable limits. One transistor in control circuit 40527-516-57 failed leakage current and the second was borderline. Both transistors showed higher than average leakage currents initially, however.

Quiescent current (I_{DD}) measurements of the CD4001 CMOS (Table 35) devices again showed decreasing leakage currents as the burn-in progressed. No failures occurred and the currents remained well below the specification requirement of <1000 nA.

As in the prior stress tests, none of the 1776 coated wire bonds failed and no device failures attributable to the coatings were identified.

Photographs of CMOS devices coated with DC-E2907-44-1 silicone and the 3:1 silicone-halocarbon mixture taken on completion of the steady state life test are shown in Figures 42 and 43. It can be seen that the wires still retain the coatings and no flow due to softening of the coatings is evident.

3.3.3.2 Insulation Resistance and Breakdown Voltage Results

The insulation resistances and breakdown voltages were measured on the circuits subjected to burn-in and steady state life testing using the thin film interdigitated capacitors with 0.00635 cm (2.5 mil) spacings and 1.429×10^{-3} squares. The insulation resistances were calculated from the measured leakage currents with 200 volts applied to the capacitors. The results are shown in Table 36. The insulation resistances of the coated and uncoated control circuits are comparable. The breakdown voltages for the control circuits averaged 460 volts while no breakdowns occurred with any of the coated circuits below 1000 volts which was the maximum voltage applied.

3.3.3.3 Hermeticity and PIND Test Results

Upon completion of the 240 hours burn-in and 1000 hours steady state life tests at 125°C, all of the packages were hermeticity tested in accordance with MIL-STD-883A, Method 1014.1, Condition A_2 and C_2. All of the packages were hermetic indicating no seal degradation under the conditions of the test. All of the circuits also passed the PIND test with the exception of one uncoated control circuit (40527-516-22). As described in paragraph 3.3.2, one control circuit also failed the PIND test after mechanical shock and constant acceleration testing. All of the circuits had passed the PIND test after sealing. A total of two out of sixteen (12.5 percent) of the

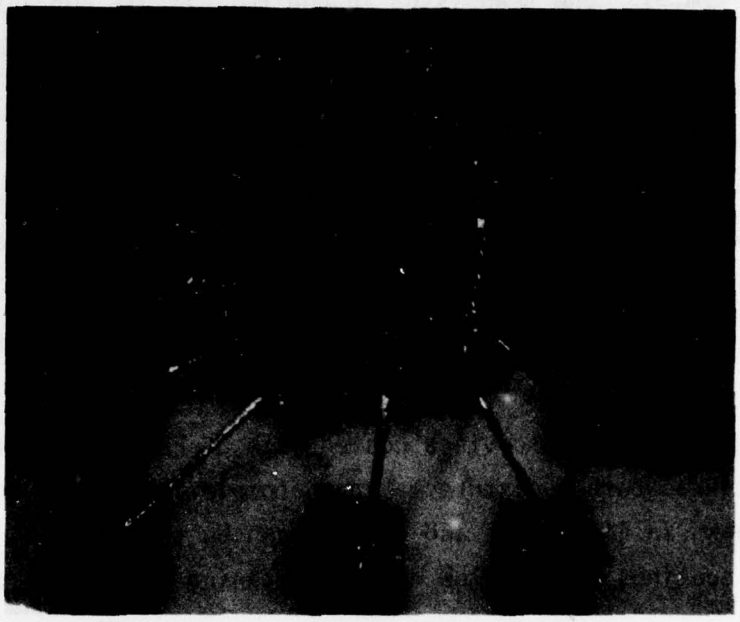

Figure 42. Photograph of CMOS Coated With DC-E2907-44-1 After Burn-In and Steady State Life Testing

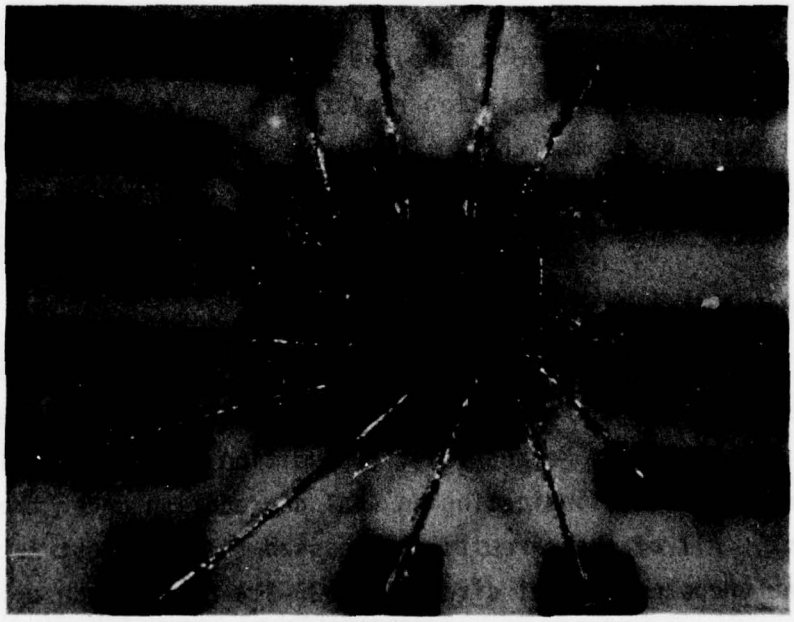

Figure 43. Photograph of CMOS Coated With 3:1 Mixture of Silicone and Halocarbon after Burn-In and Steady State Life Testing

TABLE 36. LEAKAGE CURRENT, INSULATION RESISTANCE AND BREAKDOWN VOLTAGE TEST RESULTS FOR HYBRID CIRCUITS FOLLOWING BURN-IN AND STEADY STATE LIFE TESTS

Circuit Coating	Leakage Current ($x10^{-12}$ amps)		Insulation Resistance ($x10^{13}$ ohms)		Insulation Resistivity ($x10^{16}$ ohms/square)		Breakdown Voltage (V)	
	Avg.	Range	Avg.	Range	Avg.	Range	Avg.	Range
DC-E2907-44-1	8.13	7.9 - 8.5	2.46	2.35 - 2.53	1.72	1.64 - 1.77	>1000	>1000
3 pbw DC-E2907-44-1 plus 1 pbw Halocarbon 15-00	8.19	8.0 - 8.5	2.44	2.35 - 2.5	1.71	1.64 - 1.75	>1000	>1000
Controls	8.33	8.0 - 8.5	2.40	2.35 - 2.5	1.68	1.64 - 1.77	460	440 - 480

uncoated control circuits therefore failed the PIND test as a result of the stress tests. This points out the necessity for a coating to immobilize particles which may be physically or electrostatically attached initially and later dislodged during operation of the system containing the circuits.

3.4 Material and Process Specifications

A material and a process specification covering the qualification, acceptance, processing, and control of the coating materials are contained in Appendices A and B, respectively. These specifications should be considered as preliminary and are based on the data developed in this study on the experimental coatings evaluated. Additional parametric data are required and the data shown require verification tests performed on additional lots of the material.

3.5 Environmental Impact

If the silicone coating is spray applied as a six wt % solution in toluene to yield a coating thickness of 0.0038 cm (0.0015 inch), and assuming that the area covered by the spray is five times the area of the average microcircuit to be coated, approximately two ml of coating solution will be required to coat a 2.54 x 2.54 cm (1.0 x 1.0 inch) hybrid microcircuit. Approximately two ml of toluene would therefore be released into the atmosphere during the coating and drying of an average hybrid microcircuit. If 1000 hybrid microcircuits were coated per week in a production facility, only 2 liters/week of toluene would be released into the atmosphere. This amount of toluene is not believed to be significant. However, the toluene vapors may be removed using carbon absorbers, scrubbers, or afterburners on the spray booths.

4.0 CONCLUSIONS

Based on the results of this program, the following conclusions have been drawn:

(1) Both the DC-E2907-44-1 silicone and the 3:1 mixture of DC-E2907-44-1 and the toluene extract of Halocarbon 15-00 had no adverse effects when properly applied as coatings to the hybrid microcircuit components tested in this study.

(2) The coatings do not degrade wire bonds provided that bridging between the wires or from the wires to the package or device is eliminated.

(3) The coatings can be easily removed using trichlorotrifluoroethane as a solvent in a two chamber immersion degreaser or Soxhlet extractor. Since the coatings are solvent removable, mechanical removal is neither required or desired.

(4) Wire bonds reworked after coating removal showed bond strengths comparable to the original bonds.

(5) The coatings should be spray applied to a dried film thickness of 0.001 to 0.0038 cm (0.0004 to 0.0015 inch). If bridging of wire bonds occurs, the coating should be removed and reapplied.

(6) Coatings of the above thicknesses have the ability to immobilize particles introduced into packages either before or after coating application.

(7) Electrical tests of the coated electronic circuits after 1240 hours of burn-in showed no electrical leakage effects due to the presence of mobile ions in the coatings.

(8) Outgassing from the coatings was insufficient to cause loss of hermeticity after 1000 hours at 150°C.

(9) The coatings provide excellent wetting of surfaces in hybrid microelectronic packages showing no evidence of beading.

(10) The coatings can be readily removed from package seal areas and showed no evidence of contamination of these areas either through lowering of sealing yields or loss of hermeticity during the high temperature storage and burn-in tests.

(11) The use of these coatings for particle immobilization in microcircuits permits "hands off" removal followed by standard rework and recoating procedures. While the materials are expensive, the usage is small and the cost per microcircuit will be minor. The added labor cost will also be small involving primarily the cost of coating application. The cost of coating removal prior to rework is expected to be comparable to that of a standard cleaning procedure.

5.0 RECOMMENDATIONS

As a result of this study, the effectiveness of the solvent soluble coatings in providing a solution to the particulate contamination problem in hybrid microcircuits has been demonstrated. It is recommended that the additional material and process data necessary for qualification, acceptance, processing, and control of the selected solvent soluble coatings be developed. The acceptability of the coatings should also be verified using high density production hybrid microcircuits containing a variety of devices. The coated production hybrid microcircuits should be tested for compliance with the screen and qualification test requirements of MIL-STD-883B, Class B.

APPENDIX A

MATERIAL SPECIFICATION FOR PARTICLE IMMOBILIZING COMPOUND FOR MONOLITHIC AND HYBRID MICROCIRCUITS

1. SCOPE

1.1 Scope. This specification covers solvent soluble conformal coatings which are suitable for application to monolithic and hybrid microcircuits for the purpose of immobilizing particulate contamination.

1.2 Classification. The conformal coatings shall be of the following types as specified (see 6.2):

Type I: Solvent soluble block copolymer of silicone and polystyrene resins.

Type II: Solvent soluble formulation of Type I with a polyhalocarbon.

2. APPLICABLE DOCUMENTS

2.1 The following documents of the latest issue in effect form a part of this specification to the extent specified herein:

Standards

Fed. Test Method Standard No. 141	Paint, Varnish, Lacquer, and Related Materials; Methods of Inspection, Sampling, and Testing
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
MIL-STD-883	Test Methods and Procedures for Microelectronics

American Society for Testing Materials

ASTM D149	Dielectric Strength of Electrical Insulating Materials at Commercial Power Frequencies, Tests for
ASTM D150	AC Loss Characteristics and Dielectric Constant (Permittivity) of Solid Insulating Materials, Tests for
ASTM D257	DC Resistance or Conductance of Insulating Materials, Tests for

3. REQUIREMENTS

3.1 Qualification. The material furnished under this specification shall be a product which has been tested and has passed the qualification tests specified herein.

3.2 Material Properties

3.2.1 Shelf Life. The shelf life of the material when stored in unopened containers at a temperature of 25 ± 5°C shall be a minimum of six months when tested as specified in 4.5.2.1.

3.2.2 Appearance. The material shall be clear, colorless, and free of particles when inspected as specified in 4.5.2.2.

3.2.3 Ionic Content. The ionic content of the material when tested as specified in 4.5.2.3 shall be in accordance with Table I.

TABLE I. IONIC CONTENT

	Parts Per Million, Maximum
Potassium	TBD
Sodium	TBD
Other metal ions	TBD
Chloride	TBD
Other halide ions	TBD

3.2.4 Infrared Spectrum. An infrared spectrum of the material shall be prepared in accordance with 4.5.2.4 during qualification. The infrared spectra obtained during subsequent acceptance testing shall be identical to that obtained during qualification with the exception of absorption variations due to sample thickness.

3.3 Performance Properties

3.3.1 Volume Resistivity. When tested as specified in 4.5.2.5, the volume resistivity shall be in accordance with that specified in Table II.

3.3.2 Insulation Resistance. When tested as specified in 4.5.2.6, the insulation resistance shall be in accordance with that specified in Table II.

TABLE II. ELECTRICAL PROPERTIES

Electrical Property	Requirement
Volume resistivity	$\geq 1 \times 10^{15}$ ohm-cm
Insulation resistance, 200 volts	$\geq 2.40 \times 10^{13}$ ohms
Dielectric constant, 10^2 Hz	≤2.65 (Type I) and TBD (Type II)
Dissipation factor, 10^2 Hz	≤0.0050
Dielectric strength	≥350 volts/mil

3.3.3 Dielectric Constant. When tested as specified in 4.5.2.7, the dielectric constant shall be in accordance with that specified in Table II.

3.3.4 Dissipation Factor. When tested as specified in 4.5.2.8, the dissipation factor shall be in accordance with that specified in Table II.

3.3.5 Dielectric Strength. When tested as specified in 4.5.2.9, the dielectric strength shall be in accordance with that specified in Table II.

3.3.6 Solvent Removability. The material shall be solvent removable when tested as specified in 4.5.2.10. There shall be no evidence of coating residues.

3.3.7 Weight Loss. When tested as specified in 4.5.2.11, the maximum weight loss of the material shall be as specified in Table III.

3.3.8 Thermal Shock Resistance. When tested as specified in 4.5.2.12, the wire bonds on the coated specimens shall show a minimum bond strength of 3.0 grams prior to coating and after temperature cycling, and a minimum bond strength of 2.5 grams after coating removal. If bond failures occur in the control specimens and in the coated specimens, the test shall be repeated.

TABLE III. WEIGHT LOSS

Temperature	Percent Weight Loss	
	Type I	Type II
200°C	≤0.05	TBD
240°C	≤0.10	TBD
300°C	≤0.60	TBD

4. QUALITY ASSURANCE PROVISIONS

4.1 Classification of Tests. The inspection of the material is classified as (a) qualification inspection, and (b) quality conformance inspection.

4.2 Qualification Inspection. Qualification inspection comprises those tests performed on samples submitted for approval as qualified products.

4.2.1 Sample Size: Coating materials shall be furnished in sealed containers in sufficient quantity to perform all of the examinations and tests contained in this specification.

4.2.2 Failures. Failure of one or more test specimens shall be cause for refusal to grant qualification approval.

4.3 Quality Conformance Inspection. Quality conformance inspection comprises the tests performed on individual lots which have been submitted for acceptance.

4.3.1 Test Lot. A test lot shall consist of all material manufactured under the same batch number.

4.3.2 Test Sample. A sample consisting of one or more packages shall be selected at random from each lot of material for quality conformance inspection.

4.3.3 Inspection. Inspection of the test sample to determine compliance with the requirements specified in Table IV shall be conducted in accordance with the corresponding test method paragraph.

4.3.4 Failures. Failure of one or more test specimens shall be cause for rejection of the lot.

TABLE IV. QUALITY CONFORMANCE INSPECTION

Property	Requirement Paragraph	Test Method Paragraph
Appearance	3.2.2	4.5.2.2
Ionic Content	3.2.3	4.5.2.3
Infrared Spectrum	3.2.4	4.5.2.4
Packaging and Packing	5.1	5.1
Marking	5.2	5.2

4.4 Test Equipment. The test equipment for conducting examinations and tests shall be as specified in the applicable test methods and procedures paragraphs.

4.5 Test Methods and Procedures

4.5.1 Test Specimen Preparation. Test specimen size and configuration shall be as specified in the applicable test methods paragraphs. Drying temperatures and times shall be a minimum of 1.0 hours at room temperature followed by one hour at 150 + 5°C (in a vented oven in a nitrogen atmosphere), and followed by a minimum of 4 hours at 150 ± 5°C at less than one Torr pressure. The thickness of the dried film (on flat surfaces) shall be 0.001 to 0.0038 cm (0.0004 to 0.0015 inch) unless otherwise specified.

4.5.2 Tests

4.5.2.1 Shelf Life. A sufficient amount of material in the original unopened containers shall be stored under the conditions specified in 3.2.1. At the end of the storage period, the material shall meet the quality conformance requirements specified in 4.3.3

4.5.2.2 Appearance. The material shall be visually examined in the container for conformance to 3.2.2.

4.5.2.3 Ionic Content. To be determined (TBD).

4.5.2.4 Infrared Spectrum. Sufficient material shall be applied to an infrared window to obtain a thickness of approximately 0.0254 mm (0.001 inch) when the material is dried. The material shall be dried as specified in 4.5.1, except that the vacuum bake shall not be used. The infrared spectrum shall be recorded over the wavelength range of 2.5 to 15 micrometers. The spectra shall conform to the requirements of 3.2.4.

4.5.2.5 Volume Resistivity. The volume resistivity of the material when dried and vacuum baked in accordance with 4.5.1, shall be determined in accordance with ASTM D257 for conformance to 3.3.1.

4.5.2.6 Insulation Resistance. The insulation resistance of the material when dried and vacuum baked in accordance with 4.5.1 shall be determined in accordance with MIL-STD-202 for conformance to 3.3.2.

4.5.2.7 Dielectric Constant. The dielectric constant of the material when dried and vacuum baked in accordance with 4.5.1 shall be determined in accordance with ASTM D150 for conformance to 3.3.3.

4.5.2.8 Dissipation Factor. The dissipation factor of the material when dried and vacuum baked in accordance with 4.5.1 shall be determined in accordance with ASTM D150 for conformance to 3.3.4.

4.5.2.9 Dielectric Strength. The dielectric strength of the material when dried and vacuum baked in accordance with 4.5.1 shall be determined in accordance with ASTM D149 for conformance to 3.3.5.

4.5.2.10 Solvent Removability. Two clear plate glass panels approximately 2.54 x 5.08 cm (1 x 2 inches) shall be prepared in accordance with Method 2021 of FED-STD-141. The panels shall be coated by dip or spray application and dried as specified in 4.5.1. The panels shall be placed in a Soxhlet extractor containing trichlorotrifluoroethane solvent, subjected to four extraction cycles and examined visually under 10x magnification for conformance to 3.3.6.

4.5.2.11 Weight Loss. The thermal stability of the material shall be determined to 480°C using thermogravimetric analysis (TGA). The material shall be dried and vacuum baked in accordance with 4.5.1 prior to testing. The heating rate shall be 10°C/minute in a nitrogen ambient. The weight loss shall conform to 3.3.7.

4.5.2.12 Thermal Shock Resistance. Test specimens shall be prepared using silicon devices containing a minimum of 18 aluminum metallized bonding pads (may be nonfunctional devices). The devices shall be adhesive bonded into packages containing a minimum of 18 leads. Gold wires 0.00254 mm (0.001 inch) in diameter shall be ultrasonically bonded from the package leads to the device bonding pads. A total of eight specimens shall be prepared. Six wires shall be pulled to destruction on each specimen in accordance with MIL-STD-883, Method 2011, Condition C. The remaining wires shall be nondestructively tested at 3.0 grams. The wires selected for destructive test shall be from identical locations on each specimen and should

be representative of the bonding configurations (length and dress) contained on the specimens. If any of the wires on a specimen show bond strengths less than 3.0 grams, a new specimen shall be prepared. Four of the specimens shall then be coated as specified in 4.5.1. (If the coating forms bridges between adjacent wires or from the wires to the device or package, the coating shall be removed using trichlorotrifluoroethane in a vapor degreaser or Soxhlet extractor. The specimens may then be recoated as specified in 4.5.1. The four uncoated control specimens shall be subjected to the same cleaning and drying processes as the coated specimens. The coated and uncoated control specimens shall be thermally cycled per MIL-STD-883, Method 1010, Condition C, for 100 cycles. An additional six wires on each specimen shall then be pulled to destruction. The coating shall then be removed as specified above and the remaining wires on each specimen shall be pulled to destruction to establish compliance with 3.3.8.

5. PREPARATION FOR DELIVERY

5.1 Packaging and Packing. The material shall be packaged in accordance with the standard commercial practice to assure safe delivery by common carrier and prevent contamination during normal handling.

5.2 Marking. Interior and exterior containers shall be permanently and legibly marked in accordance with standard commercial practice. Marking shall include, but not be limited to, the following information:

(a) Specification number and type
(b) Manufacturer's designation
(c) Manufacturer's lot or batch number
(d) Manufacturer's name and address
(e) Date of manufacture
(f) Net weight of contents in container

APPENDIX B

CONFORMAL COATING OF MONOLITHIC AND HYBRID MICROCIRCUITS FOR PARTICLE IMMOBILIZATION AND/OR PROTECTION

1. SCOPE

1.1 This specification establishes requirements for conformal coating of monolithic and hybrid microcircuits for particle immobilization and/or protection. The coatings applied by this process must be qualified to the Material Specification for Particle Immobilizing Compound for Monolithic and Hybrid Microcircuits (Appendix A).

1.2 The coatings have service temperatures of -65°C to +150°C in hermetically sealed packages.

1.3 The materials are intended for use as a coating having an average thickness of 0.0100 mm to 0.0380 mm (0.0004 to 0.0015 inch).

1.4 The coatings are readily removed from coated surfaces with trichlorotrifluoroethane. As a consequence, the coated microcircuit should not be exposed to this solvent unless devices and/or wire bonds require rework. When rework is required, the coating can be completely removed with trichlorotrifluoroethane, and devices and/or wire bonds can be replaced and/or rebonded using the same techniques and materials that were originally used in the assembly of the monolithic or hybrid microcircuit.

1.5 These coatings will dissolve in aromatic solvents such as toluene and xylene. Use of other solvents on these coatings should be evaluated before exposing coated microcircuits to the particular solvent.

2. DOCUMENTS, MATERIALS AND EQUIPMENT

2.1 Applicable Documents

The following documents of the latest issue in effect, except as otherwise indicated, form a part of this specification to the extent specified herein. In the event of conflict between documents referenced herein and the contents of this specification, the contents of this specification shall supersede.

MIL-STD-883B	Test Methods and Procedures for Microelectronics
Appendix A	Material Specification for Particle Immobilizing Compound for Monolithic and Hybrid Microcircuits
FED STD 141	Paint, Varnish, Lacquer and Related Materials: Methods of Inspection, Sampling and Testing

2.2 Materials

Type I coating, silicone, per requirements of Appendix A
Type II coating, silicone and halocarbon mixture (3 to 1, respectively) per requirements of Appendix A
Toluene, TT-T-548 or Reagent Grade (ACS)

Trichlorotrifluoroethane, MIL-C-81302, Type I or Type II
Trichlorotrifluoroethane-acetone azeotropic mixture, Freon TA or equivalent
Isopropyl Alcohol, TT-I-735, Grade A or Reagent Grade (ACS)
Methyl Ethyl Ketone, TT-M-261, or Reagent Grade (ACS)
Electrical Tape; Permacel No. 422, or equivalent

2.3 Equipment

Cotton swabs
Conventional artists air brush spray equipment, such as PAASCHE, Model No. HS #3 or equivalent
Paint hood for spray exhaust and solvent evaporation with activated carbon filters to trap volatile organics, or equivalent exhaust system
Vented oven with dry nitrogen atmosphere, equipped with N_2 purging
Vapor-distillate-spray degreaser, liquid-vapor degreaser, or equivalent

Vacuum chamber capable of maintaining 150°C temperature and pressure of less than 1 Torr

Aluminum foil

Masking fixture for packages to be coated

Soxhlet, or Soxhlet type, extraction equipment and/or vapor degreaser (vapor-distillate spray or equivalent)

3. REQUIREMENTS

In the event of any conflict between the requirements of this specification and drawings calling out this specification, the requirements of the drawing shall take precedence.

3.1 Unless otherwise specified, the tolerances on weights and measures stated herein are absolute. Calibration errors have been taken into account in specifying tolerances.

3.2 All materials and chemicals required by this specification shall be handled, used, and stored in accordance with existing environmental and safety procedures as required at the facility, or facilities, where the coating is applied.

3.3 All wire bonds shall have passed nondestructive pull tests in accordance with the applicable procurement document for the microcircuit. Wire bonds shall show visible stress relief in accordance with good workmanship practices. Prior to coating, all microcircuits shall meet the requirements of preseal visual screen of MIL-STD-883 for Class B microcircuits.

3.4 Handling and Storage

3.4.1 Assemblies and/or devices that are sensitive to electrostatic charges shall be handled and stored in accordance with existing requirements at the facilities where the microcircuits and devices are produced.

3.4.2 Cleaned assemblies shall be protected from dust and recontamination at all times. Coated, but unsealed,assemblies shall also be protected. When not in process, unlidded devices shall be stored in containers with a nitrogen pressure above ambient; i.e., slight positive flow.

3.5 Cleaning Prior to Conformal Coating

3.5.1 All assemblies shall be cleaned prior to conformal coating. Cleaning shall be accomplished in a vapor degreaser or in a Soxhlet, or Soxhlet type, extractor using either the azeotropic mixture of trichlorotrifluoroethane-acetone, or trichlorotrifluoroethane alone if the azeotropic mixture is incompatible with materials in the microcircuit.

3.5.1.1 Vapor Degreasing

(a) Rack parts to be cleaned and suspend in the vapor condensation area above the boiling sump containing the degreasing solvent. Maintain in position until solvent ceases to run off surfaces of parts, but not less than 1.5 nor more than 3.5 minutes.

(b) Transfer the rack and parts to condensate tank, immerse in flowing condensate for 1 to 5 minutes.

(c) Return rack and parts to vapor area above boiling sump and leave in condensing vapors for 1 to 5 minutes or spray with fresh condensate for 1 to 5 minutes.

3.5.1.2 Soxhlet Cleaning

Rack parts in extractor part of Soxhlet, or Soxhlet type, extractor of appropriate size. Parts shall be cleaned with a minimum of six extraction cycles.

3.5.2 The basic cleaning bath shall be maintained to provide a water-free trichlorotrifluoroethane-acetone azeotropic mixture (or trichlorotrifluoroethane alone) in the vapor phase. Liquid in the boiling sump shall be maintained so that water, acids, and insoluble impurities are prevented from harming any equipment or devices and/or assemblies. Procedures and limits on contaminants may be found in the various suppliers' literatures; e.g., DuPont Freon TA, Freon TF and Freons.

3.5.3 After cleaning, all assemblies shall be examined for foreign particulate matter in accordance with the requirements of the preseal visual screen of MIL-STD-883, Class B microcircuits. Assemblies with contamination shall be recleaned until the assemblies are free of foreign particles. Loose particles may be removed with an air brush with 10 to 30 psig nitrogen line pressure with caution, so that the wires will not be disturbed or deformed.

3.6 Masking

3.6.1 Coating shall not be applied to the sealing flange of the package, nor to the outside of the package (especially package leads). Packages can be mounted in a masking fixture for the particular package so that the sealing flanges will be flush with the surface of the masking fixture. Packages can be secured by applying another fixture to mask the package flanges, or by applying masking tape (e.g., Permacel No. 422) over the flange surfaces. Avoid stretching the tape during its application. The tape shall be firmly pressed into position. The backside of the masking fixture shall protect the rest of the packages from coating. If static sensitive devices are present, all package leads should be electrically grounded, as well as protected from coating application. All packages shall be securely mounted in the masking fixtures prior to and during coating operations.

3.6.2 Parts shall be protected from any contamination during masking, coating, baking, or other operations until the packages are sealed.

3.7 Conformal Coating Application

3.7.1 Material: The conformal coating materials shall conform to the requirements for Type I or Type II coatings as specified in Appendix A, and the assembly specification and/or drawing.

3.7.2 These materials contain a volatile solvent, toluene, and the containers shall be kept tightly sealed, except when transferring contents, to prevent solvent evaporation. The opened containers shall be protected from contamination and humid environments. The solids content of the coating shall be checked before adding toluene for thinning the coating or, as an alternative, the viscosity of the thinned coating shall be in the range of a solution containing 6.0 to 6.6% silicone (with or without halocarbon, as applicable).

3.7.3 For coating with both Type I and Type II materials, the silicone content shall be between 6.0 and 6.6 weight percent. Type II coating shall be mixed, before thinning of the silicone, with halocarbon solution so that the weight ratio is 3.5 - 3.0 pbw silicone to 1.0 pbw halocarbon. The mixture can then be thinned with toluene to bring the silicone

content to between 6.0 and 6.6 percent. The 6.0% silicone concentration is generally easier to spray and has a decreased amount of cobwebbing in the back spray.

3.7.4 Spray Application

3.7.4.1 Electrostatic sensitive devices or assemblies shall have their leads grounded during the coating process. The spray gun, or brush, used for coating shall be metallic and connected to the same ground as that used for microcircuit leads.

3.7.4.2 A test substrate shall be attached to each masking fixture during coating application so that the coating thickness can be verified. The test substrate shall have been cleaned by the same process as used for cleaning the parts to be coated. Each test substrate shall be marked to identify the microcircuits that it represents.

3.7.4.3 With the masking fixture at 70 to 90 degrees with the horizontal plane, apply coating by making one or more passes over the uncoated area of the assembly. The nitrogen line pressure used for spraying should be no more than 30 psig. The air brush distance and pressure must be adjusted to allow coating without disturbing the position of the wires. Rotate masking fixture 90° two more times with spray application each time. Immediately, turn masking fixtures upside down and air dry for 30 minutes minimum.

3.7.4.4 After air drying, the coated microcircuits and/or devices may be examined for the following:

(a) Wires shall not be deformed.

(b) Determine coverage of coating on leads, devices, and substrate. Devices with a porous ceramic body may not show any coverage of coating because of absorption and the ceramic area can be disregarded with respect to coating coverage.

(c) The thickness of coating on leads can be determined visually at this time by comparing coating thickness with the wire diameters or by using a reticle. If coating thickness of Type I coating is 0.013 to 0.0254 mm (0.5 to 1.0 mils) do not apply a second coat.

If coating thickness of Type II coating is 0.018 to 0.0254 mm (0.7 to 1.0 mil), do not apply a second coat. If coating on the leads is not sufficiently thick, apply second coat using the same procedure as in the original coating of the microcircuits.

(d) Examine wires to insure that they are not bridged with coating to devices, substrate, or other objects. Normal coating fillets near wire attachment are desirable and acceptable. Parallel (common) wires that are used for making the same electrical connection and are within 0.076 mm (3 mils) of each other may be bridged; this condition is acceptable provided the wires show stress relief. If only a few wires are bridged, coating may be cut between wires with fine surgical scissors, being careful not to disturb wires. Coating can also be removed by the procedure in paragraph 3.8. Fine coating cobwebs between wires and devices are acceptable, maximum diameter of 0.013 mm (0.5 mil), and will normally disappear on subsequent baking operations. See Quality Assurance Provisions for limits on cobwebbing and fine strands after initial 150°C bake.

(e) Because the coating is clear and colorless, the direction of the light source or reflected light will sometimes have to be adjusted in order to make the coating visible on the wires, especially when gold wires are over gold surfaces.

3.7.5 Demasking

Remove masking tape, if used, from package flanges. Remove packages from fixtures. Clean all sealing flanges with a toluene moistened lint-free cloth, paper, or cotton swab. Clean until sealing flanges are free of coating, masking tape residues, or any other foreign material. Remove any adhesives on the flange with a methyl ethyl ketone-moistened cotton swab, lint-free cloth, or paper. If necessary, use approved tools for scrapping adhesive off of sealing flange, followed by cleaning with a MEK moistened swab. Allow to dry (10 minutes minimum) before any baking operation.

3.7.6 Initial 150°C Bake

Prior to baking of coated assemblies, or devices, verify maximum temperature to which unpowered devices can be exposed. If maximum temperature

is less than 150°C, obtain alternate baking parameters from the engineer responsible for the particular part. Bake coated microcircuits in vented 150°C ± 5°C oven with a nitrogen atmosphere for one to two hours. Before placing microcircuits in oven purge oven with increased amount of nitrogen flow so that atmosphere in oven, after opening and closing, will be all nitrogen within five minutes of closing oven door. Reduce nitrogen flow after purge to insure positive flow and nitrogen atmosphere. Position parts upside down while in oven. Assemblies may be functionally tested after they are removed from oven.

3.7.7 Vacuum Bake

3.7.7.1 If the microcircuits were functionally tested after the initial 150°C bake, reclean sealing flanges with a 50-50 mixture of isopropyl alcohol and toluene. Package lids shall be cleaned using the same procedure as specified in paragraph 3.5 and shall be stored in a nitrogen atmosphere in a cabinet with a slight nitrogen flow.

3.7.7.2 The coated microcircuits and lids shall be baked at 150 ± 5°C at a pressure ≤1.0 Torr for four hours minimum (see precautionary maximum temperature remarks in 3.7.6). The vacuum oven shall be pressurized to one atmosphere with dry nitrogen or a dry nitrogen-helium mixture and the microcircuits transferred to the dry box for sealing while still maintained in the dry ambient.

3.8 Removal of Coating from Microcircuits and Monolithic Devices

Coatings shall be removed from microcircuits and monolithic devices in accordance with 3.5, with the following exceptions:

3.8.1 The solvent shall be trichlorotrifluoroethane and shall be controlled per the manufacturer's directions.

3.8.2 Vapor Degreasing

Use procedure as specified in 3.5.1.1, except the time in the condensate tank shall be approximately 10 minutes for each 0.013 mm (0.5 mil) of coating thickness, or as necessary until coating is completely removed.

3.8.3 Soxhlet Extraction of Coating

Rack parts in extractor part of Soxhlet (or Soxhlet type) extractor of appropriate size. Remove coating using a minimum of four extraction cycles of fill and drain of the cleaning solvent per 0.013 mm (0.5 mil) of coating thickness, or as necessary until coating is completely removed. There will be some variation due to position of part in Soxhlet, and whether or not condensate is draining directly onto part.

3.9 Rework of Parts After Coating Removal

Rework of wire bonds and devices shall be in accordance with the procedures used for uncoated devices. All reworked wire bonds shall be nondestructively pull tested to the values specified in the procurement document for the microcircuit. After rework is completed, reclean and recoat per this specification.

4. QUALITY ASSURANCE PROVISIONS

4.1 All microcircuits shall meet the requirements of MIL-STD-883, Internal Visual for Class B microcircuits, before and after coating, except for the presence of coating. Method 2017 shall be used for hybrids and Method 2010 shall be used for monolithic devices. All wire bonds shall be nondestructively tested prior to coating and shall meet the minimum requirements as specified in the procurement (or in-house) wire bonding specifications.

4.2 Unless otherwise specified by drawing or assembly documents, the conformally coated microcircuit prior to vacuum baking shall meet the following minimum requirements.

(a) Thickness of the coating on the test substrate shall be between 0.010 mm (0.4 mil) and 0.038 mm (0.0015 inch).

(b) Coating thickness on the wires shall be no greater than 1-1/2 times the wire diameter.

(c) No bridging of coating, except as specified in 4.3(f) and 4.3(g), between wires, wires and devices, wires and package posts, or wires and substrate when viewed under x30 magnification. Bridging of parallel wires (common) which are apart 0.076 mm (3 mils), or less, is acceptable provided the wires show stress relief. Normal filleting of coating at the bond sites is acceptable.

(d) No evidence of disturbed or deformed wires.

(e) No evidence of coating, adhesives, or other contaminants on the sealing flange and external leads of the coated packages when viewed under x 30 magnification.

(f) All exposed conductive adhesive shall be coated.

4.3 The following coating anomalies are acceptable and shall not be cause for rework:

(a) Absence of coating or voids in the coating on the package floor or on the inner sidewalls of the package.

(b) Runs, sags, or bubbles less than 0.03 mm (0.10 mils) in diameter or in the largest dimension.

(c) Apparent lack of coating on nonconductive areas of devices with porous bodies; e.g., chip capacitors.

(d) Bridging on parallel (common) wires which are 0.0076 mm (3.0 mils), or less, apart, provided the wires show stress relief.

(e) Normal coating fillets between wires and substrates or devices at the bonding sites.

(f) Cobwebs and/or strands, of coating between wires, wires and devices, wires and substrate, wires and package posts, package post to package post provided that the coating cobwebs, or strands, are less than 0.013 mm (0.4 mil) in diameter and number no more than six for each wire (common wires excepted).

(g) A maximum of one strand of coating, up to 0.025 mm (1.0 mil) diameter between adjacent wires is acceptable provided both wires show signs of stress relief and there is no additional cobwebbing joining these wires.

4.4 At the discretion of Quality Assurance, coating thickness may be measured on test substrates after vacuum bake, but before the packages are sealed. Thickness shall be measured as stated in FED STD 141. Coating thicknesses for both Type I and Type II coatings shall not be less than 0.010 mm (0.40 mil) nor greater than 0.380 mm (1.5 mils). Packages that the failed test substrate represents shall be reworked in accordance with this specification.

REFERENCES

1. S. D. Robertson, K. L. Perkins, J. C. Monson, and J. J. Licari, "Manufacturing Methods and Technology for Screening of Electronic Components," MIRADCOM Report No. 76-3224, Contract No. DAAK40-76-C-1117, May 1978.

2. B. L. Weigand and J. J. Licari, "Polymer Adhesives Used in Hybrid Microcircuits," Research and Development Technical Report, ECOM-76-1310-F, Contract No. DAAB07-76-C-1310, May 1978.

3. J. K. Whittington, "Microcircuit Packaging Free of Loose Metallic Particles," Second Quarterly Report, Contract No. F33615-76-C-5273, 1 March 1977.

4. J. Ekmanis and S. Church, "Simple Test of Incoming Resins Rates Batch-to-Batch Quality Level," Plastic Design and Processing, 17, (3) p. 30, March 1977.

*U.S.Government Printing Office: 1979 — 657-002/494